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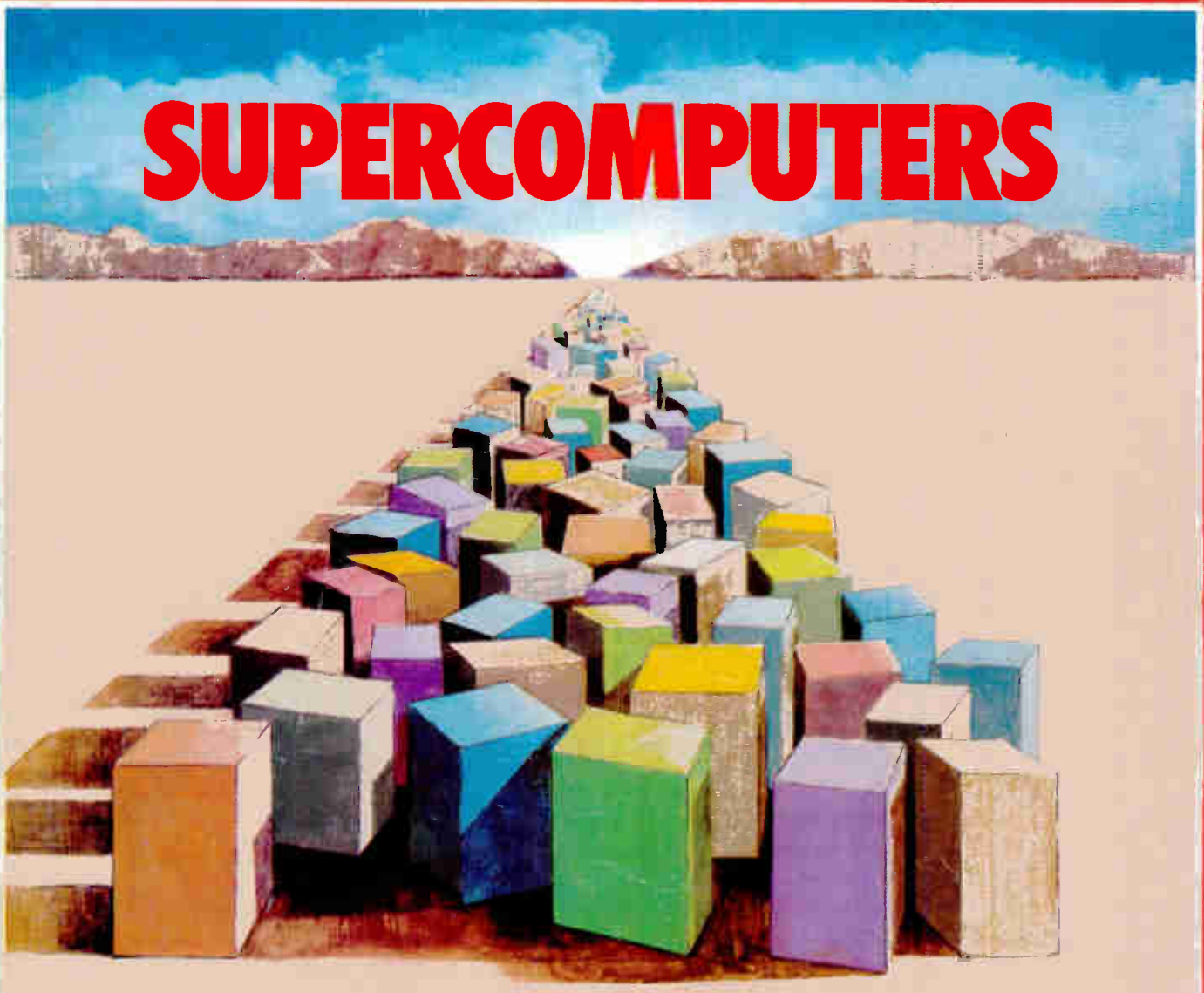

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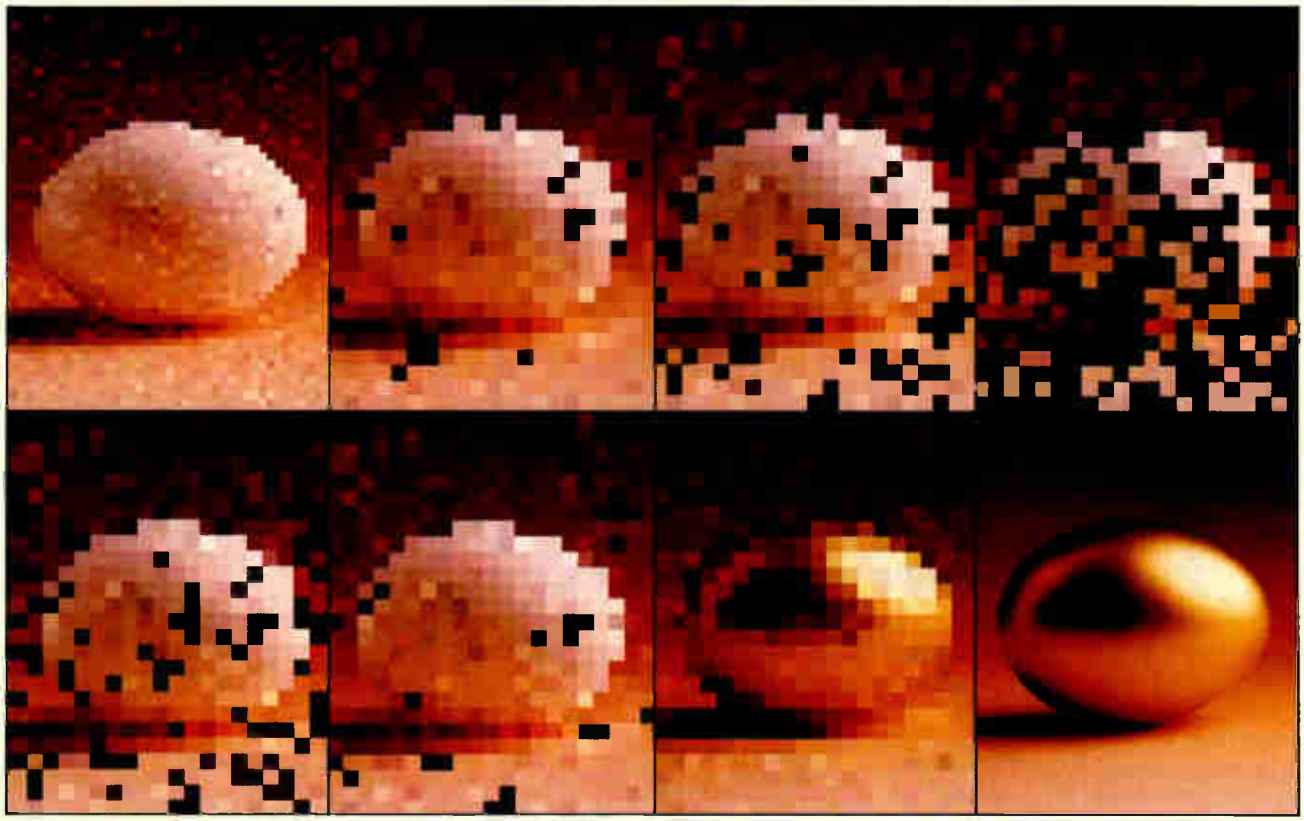

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PUBLISHER'S LETTER

In the Chinese calendar, this is the Year of the Dragon. In the annals of data processing, this year's Dragons are supercomputers; and we take a comprehensive look at this fast-evolving species and its fast-changing habitat in this special issue.

Not surprisingly, the man behind this special issue (it starts on p. 51) was computer editor Tom Manuel. Last fall, in his relentless rounds of computer makers, Tom learned that the supercomputer sector was seething. "New architectures, new software, and new technologies like gallium arsenide and HEMTs [high electron-mobility transistors] have touched off the throes of change," he says, "and a rash of new machines is on the way. Once it was just Cray [Research Inc.] and CDC [Control Data Corp.]... and multimillion-dollar price tags. Now there are 31 players in the business and single-user machines selling for under $100,000 are on their way." Two new single-user machines, in fact, debut in this issue. One is the series 10000 personal supercomputer from Apollo Computer Inc. (p. 69). "It's the first work-station system with true 64-bit architecture and the price is right—some $10,000 a megaflop," Tom says.

Manuel: "New architectures, software, and technologies."

The Apollo machine also stands out as one of the first two multiprocessor work stations to have a reduced-instruction-set architecture. It shares that distinction with a single-user supercomputer—the Titan—from Ardent Computer Corp. (p. 65). "This is a new breed, a graphics-oriented supercomputer, and the top price for the line is just $150,000," Tom notes.

Tom has found ferment as well in the middle to upper range of supercomputers. "Convex [Computer Corp.] has moved well upscale from the minisupercomputers it pioneered. Its new machines make a tenfold jump from the first machines (p. 59)." Yet another big machine getting its first public airing in the special issue is the Megaframe Supercluster, a parallel processor from the West German firm Parsytec GmbH.

All told, Tom says, "This is a monster issue, a package with an overview special report, a full-page chart that covers 65 supercomputers on the market now, two mini special reports, five technical articles, and four company profiles. It was the most challenging assignment I've had since I came aboard *Electronics* eight years ago."

To meet the challenge, Tom mustered nearly all of our editorial resources in the kind of globe-spanning effort that has long been a hallmark of *Electronics*. Field staffers throughout the U. S., in Frankfurt, and in Tokyo all made substantial contributions. A leg up came from software editor Jeremy Young, who wrote the mini special on supercomputer software (p. 75) and edited the one on Japan written by Tokyo bureau chief Charlie Cohen.

"When we first talked about the project," Jeremy says, "I wondered who in the world would buy low to midrange supercomputers. But after doing the reporting, I became convinced there's a solid market for them. Applications are waiting everywhere—in the auto and aircraft industries, in financial modeling, in film animation, in new areas of computational physics, and in interactive graphics-oriented simulation."

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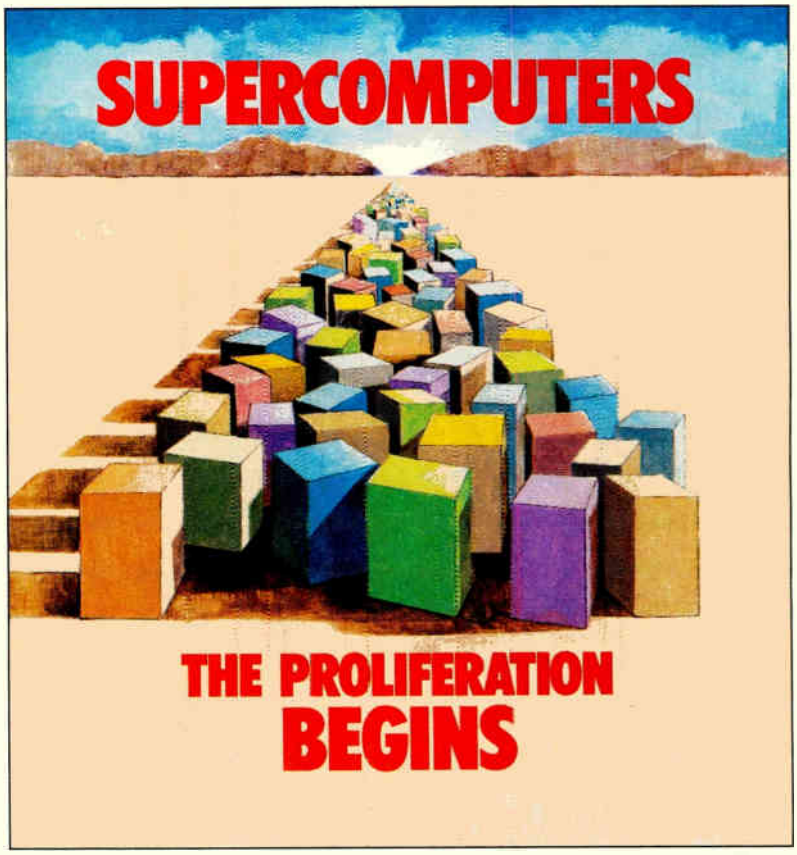

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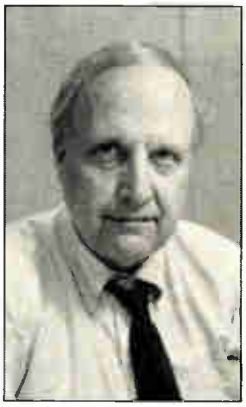
DON'T WRITE OFF THE U. S. IN MEMORY CHIPS!

The Japanese may own the dynamic RAM world, but the Americans are taking the lead in what ultimately may be the more important technology



Don't be too quick to write off the Americans in semiconductor memories—a business that's by far the biggest chip market going these days. The longer-term memory picture is definitely turning brighter for U. S. chip makers. This dramatic turnabout wasn't the subject of any paper or panel at the recent International Solid State Circuits Conference. But it was the biggest story, as far as senior technical editors Sam Weber and Stan Runyon were concerned, at a meeting they had already labeled the strongest ISSCC ever.

It seems clear that American memory technology now has a good shot at making a surprising and perhaps overwhelming comeback. While many foreign governments and corporate giants were investing hundreds of millions of dollars in chip plants to turn out millions of low-cost, low-profit dynamic RAMS, several U. S. semiconductor houses have been working quietly for several years to develop a new kind of memory that now stands an excellent chance of eclipsing the dynamic RAM's influence on computer design.

The potential of this new challenger, called the flash memory, is staggering (see p. 47). If the new class of memory moves into volume production as expected—and there seem to be few technological reasons for it not to—it will be denser, maybe faster, and more reliable than any other type of semiconductor memory. Flash memory not only will restore the memory-chip leadership to the U. S. if it pans out as we think it will, but also will radically alter computer architecture. It will likely displace magnetic disks for program storage as well as allow computers to be designed with all nonvolatile memory. The potential of the dense flash memories is so vast that Intel, which has been working hard on flash processes for four years, has decided to fold its triple-poly EEPROM program and concentrate instead on flash.

Flash may also be arriving just in the nick of time. Despite the glamour of reaching 16-Mbit parts, the dynamic RAM is running out of steam in density improvement. Trench capacitors and other processing and circuit tricks are troublesome and require painstaking care in processing. Flash memories, on the other hand, can be made with one-transistor cells, are highly scalable, and do not need elaborate engineering. While the Japanese may own the dynamic RAM world, the U. S. is in a strong position to take the lead in what ultimately may be the more important memory technology. **ROBERT W. HENKEL**

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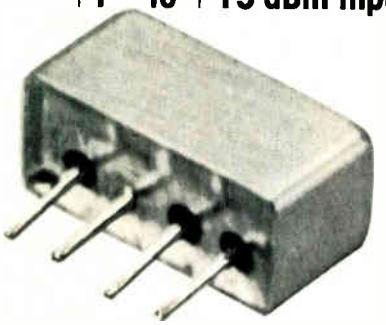

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F3	−40	−30
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For complete specifications and performance curves refer to the 1980-1981 Microwaves Product Data Directory, the Goldbook or EEM.

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LETTERS

No twisted pairs for Smart House

To the editor: A letter to the editor [*Electronics*, Oct. 1, 1987, p. 10] from Ralph Cameron expressed concern regarding the "smart-house concept," which "views shielded twisted-pair wire as being capable of carrying multiplexed control, audio, and video signals up to 1-GHz bandwidth." I did not see the article from which he extracted this information, but I would like to say that we are not considering twisted pairs (either shielded or unshielded) for anything near 1 GHz. Our plans are to use a multiconductor cable with more traditional frequency utilization.

I realize that "smart house" has become a very generic phrase and our project may not have been that to which Mr. Cameron referred. However, I wanted to offer these clarifications to avoid confusion relative to the Smart House Project.

Charles E. Gutenson
Vice President, System Integration
Smart House, Upper Marlboro, Mass.

☐ Ralph Cameron, chairman, EMI Committee, Canadian Amateur Radio Federation, Canada, replies: *The smart-house presentation by Thomas Bowling from Bell Northern Research Co. to a group of Toronto businessmen in 1986 indicated that spectrum allocation for services encompassing low-speed data control, audio, and high-speed data were to be carried on twisted-pair cable. The Canadian Amateur Radio Federation was willing to work with Mr. Bowling in investigating problems relating to radio interference as a proximity effect in urban areas. I am pleased that Mr. Gutenson reassured me that twisted-pair cable was not being considered.*

Figuring gigaflops

To the editor: The story titled, "Seymour Cray Puts the Heat On Supercomputer Rivals," [*Electronics*, Oct. 1, 1987, p. 21] reads: "Cray 4 . . . will rely on . . . 64 processors and 1-ns cycle times to achieve 128 gigaflops." According to my calculations, the Cray 4, at above configuration, should have ½-ns cycle time to achieve speed of 128 gigaflops. Am I right?

Theodor Mostsinsker
Electro-Mechanical Division
Northrop Corp., Anaheim, Calif.

☐ Christopher Hsiung, chief application engineer and high-speed computing specialist at Cray in Chippewa Falls, Wis., replies: *"Flops are calculated at two per clock; that is, one floating-point add and one floating-point multiply per cycle. Another method of increasing flops without boosting clock speed is to build additional pipelines into each CPU, with each performing an add and a multiply every cycle."*

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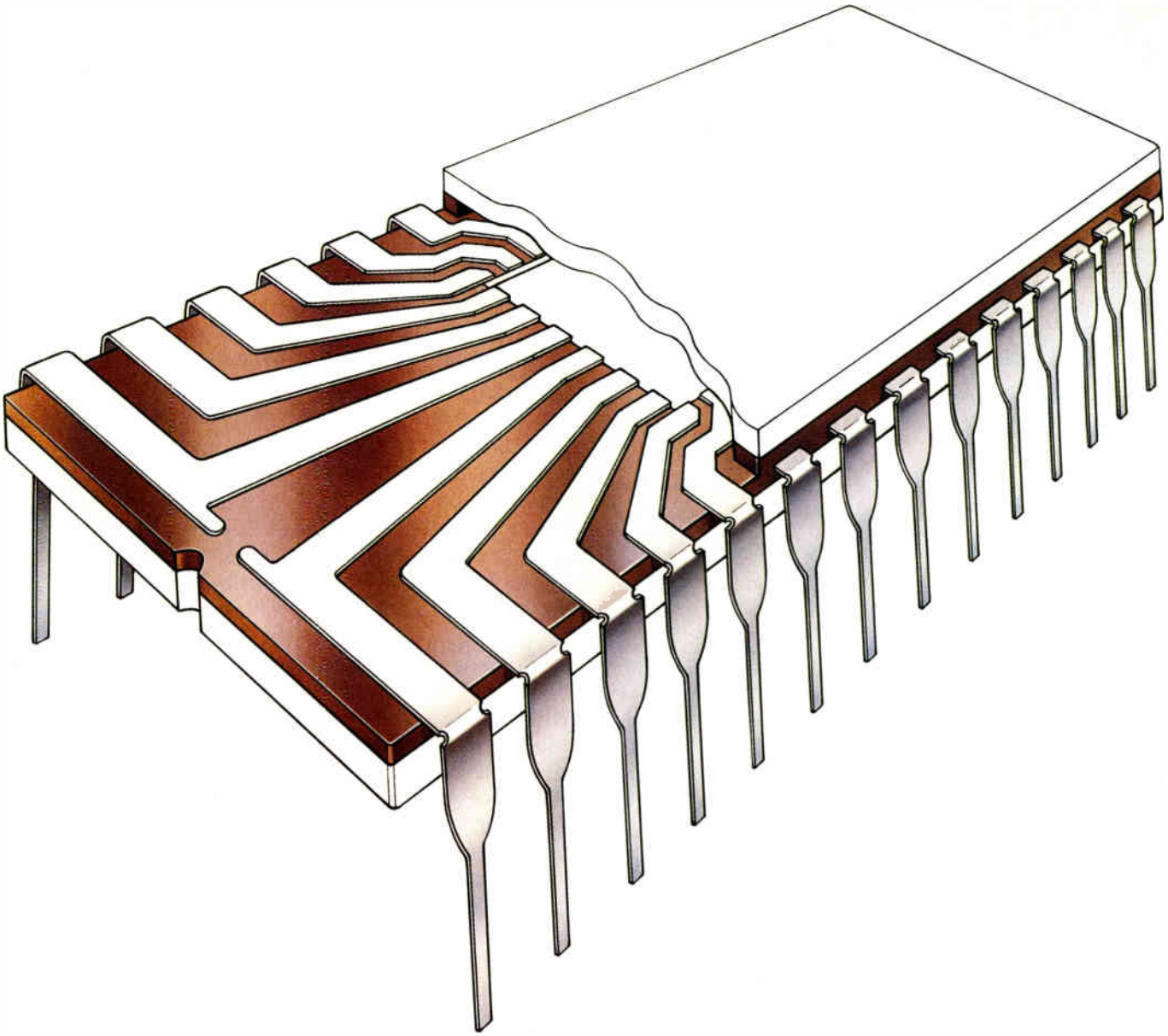

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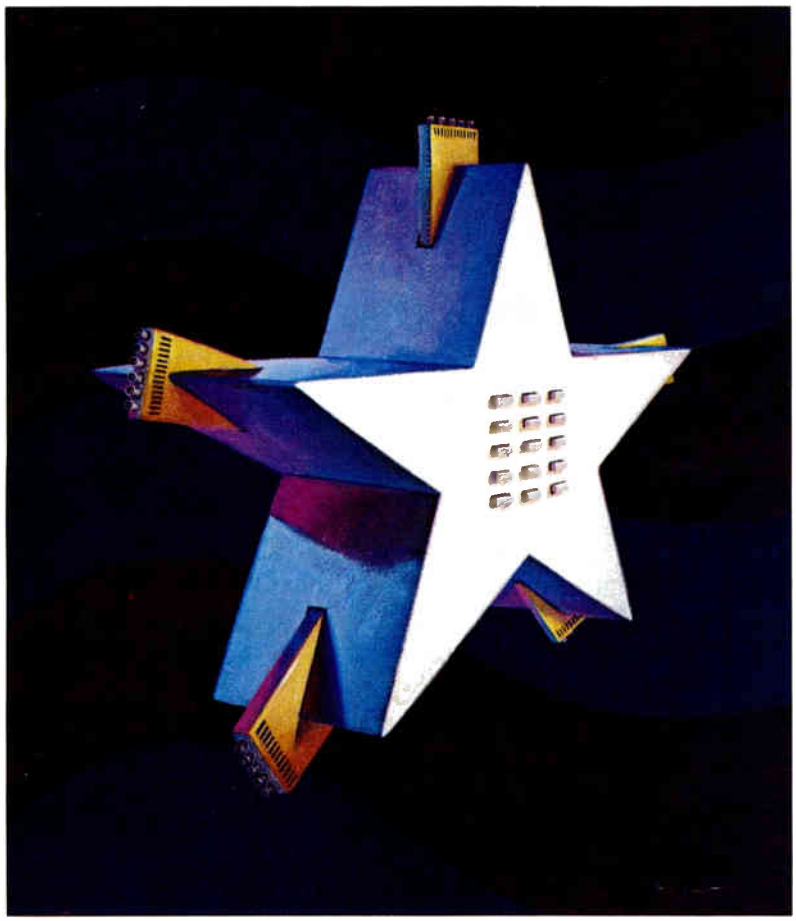
RISING STAR.



The instrument cards from Wavetek plug vertically into a VMEbus backplane and are controlled by the microprocessor.

Wavetek's Card-Based System Could Set An ATE Standard.

"A young contender is pushing its way to the forefront of the emerging market for instruments on cards. The 680 system from Wavetek Corp. uses cards in a package that can replace a rack of conventional instruments—and Wavetek's approach is already making a strong bid to become a de facto standard in its market.

Wavetek has been joined by Racal-Dana and Datron in a campaign promoting the 680's design as a standard for high-performance, instrument-on-a-card systems. If successful, it could make Wavetek a major player in the instrument-on-a-card segment of the ATE market—particularly the military segment, where growth has been hampered by a lack of standards..."

Excerpted from an exclusive article in the April 16, 1987 issue.

Electronics

THE LEADER IN NEW TECHNOLOGY COVERAGE

World Radio History

PRODUCTS NEWSLETTER

MICRO CHANNEL PROTOCOL OFFERED ON-CHIP FOR EASIER INTERFACING

PLX Technology Inc. is making it easier for system designers to cope with the complex interface for IBM Corp.'s Micro Channel by putting its protocol logic on-chip. The CMOS MCA1200 is a programmable-logic-array-based chip with powerful 24-mA drivers. It combines a 600-gate EPROM array that makes customizing easy and all the input/output buffers needed for the Micro Channel interface. The chip can replace up to 15 discrete devices and handles the functions of bus-control master, bus requester, and local arbiter, which takes care of either single-cycle or burst-data transfer requests. Using standard PLD-design software, users can customize the MCA1200 to implement additional signals through the control logic on the chip, change the function of pins, or change the protocol execution algorithm. Available in the second quarter of this year, sample pricing is $26 each. □

MATRA HARRIS'S LOW-POWER STATIC RAM RUNS TWICE AS FAST AS THE COMPETITION

Designers of military, avionic, and portable-computer equipment that demand high-speed memories with low standby power can use Matra Harris Semiconductors SA's new 64-Kbit static random-access memory to get up to twice the speed of the competition's chips. The commercial version of the 8-K-by-8-bit 65664 boasts 45-ns access times and 10-μA standby currents. Matra Harris did it by teaming its 0.8-μm Super CMOS process with a six-transistor-per-cell design. Competing six-transistor-per-cell memories have similar standby power but run at 70 to 90 ns. Competing four-transistor-per-cell memories run at 35 to 45 ns but eat up 1,000 times the power. A military version offers 50-μA standby current and 55-ns access times, and the Paris-based company will also offer 64-K-by-1-bit and 16-K-by-4-bit architectures. Samples will be available in the second quarter; pricing is not set. □

TI TAILORS PROGRAMMABLE LOGIC DEVICE FOR FAST ADDRESS DECODING

Designers can squeeze more performance out of their memory systems with a programmable address decoder from Texas Instruments Inc. The user-programmable TIBPAD16N8-7 is an application-specific programmable-logic device that simultaneously switches two inputs—a common operation in memory address decoding—in just 7 ns, which is several nanoseconds faster than competitive generic parts. The nanoseconds saved can be used to reduce the cost of the system's memory chips—low-speed chips can be substituted for fast ones without degrading system performance. The chip is similar to a generic 16L8 programmable-array-logic device from Monolithic Memories Inc., Santa Clara., Calif., but has been optimized for speed in memory-addressing applications by eliminating unneeded circuits. The 20-pin PAD is available this month, priced at $9.39 each in 1,000-piece quantities. □

PHILIPS'S PRE-AMP ON A CHIP CUTS COST AND BOARD SPACE

By integrating a complete audio-frequency pre-amplifier on a chip, Philips is delivering car-radio designers a 10% to 15% saving on component costs and a 33% saving on board space. The TEA6300 eliminates bulky, expensive, and noisy potentiometers by implementing a new switched operational-amplifier principle. A microcontroller scans the inputs from push-button switches and generates address and data words. The address and data words are fed to control circuits via the Dutch company's on-chip I^2C bus. The TEA6300, which can also be used in home high-fidelity systems, comes in a 28-pin dual in-line package or in an SO-28 minipack for surface-mount assembly. Samples are available now. Volume purchases will be delivered within 12 weeks. Price is around $10 each in 10,000 to 25,000 units. □

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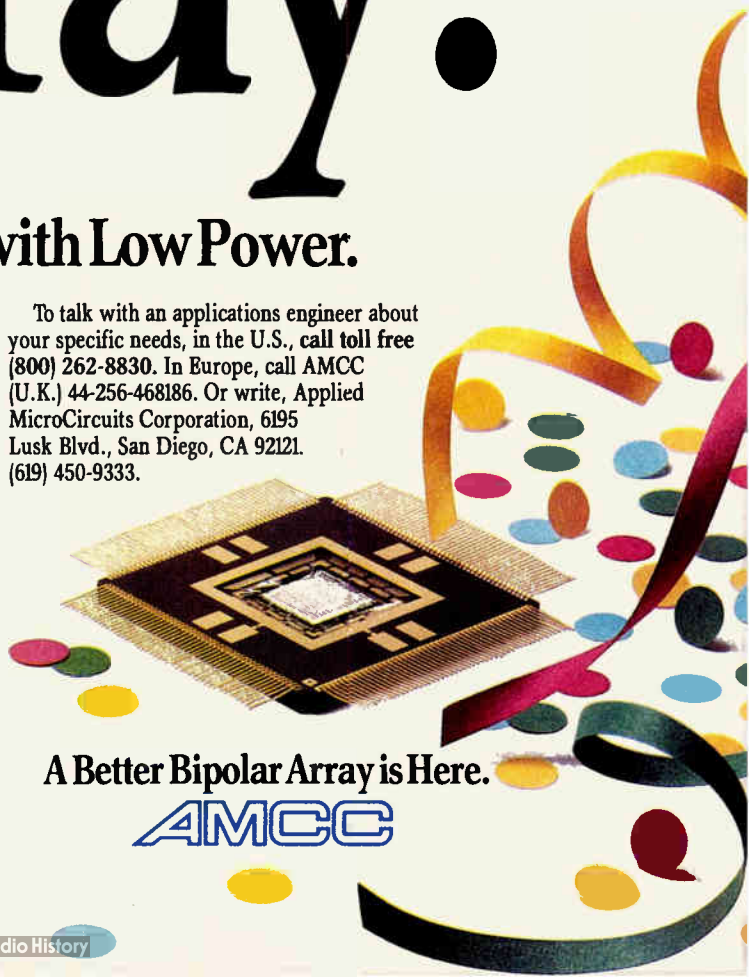

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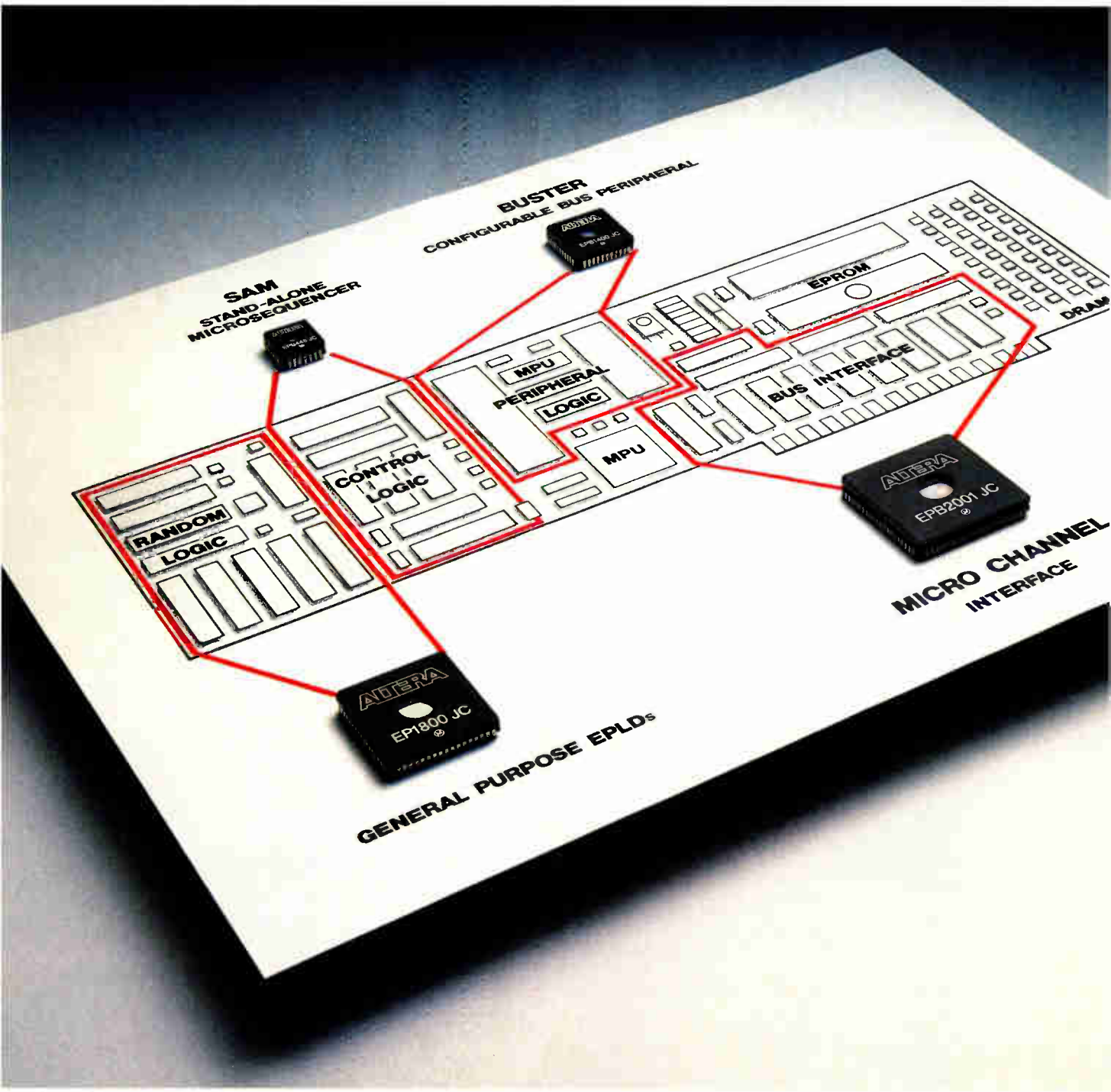

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World Radio History

Electronics

PRICES AND LEAD TIMES SOAR AS SHORTAGES GROW IN DYNAMIC RAMs

PRODUCTION SHORTFALL WILL GET EVEN WORSE AS CAPACITY IS SLOW TO BUILD

MOUNTAIN VIEW, CALIF.

The shortage of dynamic random-access memories may get worse before it gets better. Even as the scarcity of 256-Kbit and 1-Mbit chips pushes DRAM prices into a giddy climb, panicky system houses are scrambling for what were once parts galore.

In 256-Kbit parts, for users that buy from distributors— including the spot market—prices and delivery lead times are going out of sight, climbing from $1.80 and immediate delivery a year ago to $4.50 and up to 20 weeks' wait today (see table). For the big equipment houses buying large quantities direct from manufacturers, prices have risen in recent months to above $3 from just under that mark, say U.S.-based suppliers. And for 1-Mbit parts—just reaching the market and difficult to get—some users report January's $24.50 has become February's $28.50.

"Frankly, I think the supply-demand situation is going to get a whole lot worse," says John Marck, vice president and general manager of the Memory Product Division at NEC Electronics Inc. in Mountain View, Calif. Marck says the industry's first-quarter 256-Kbit shortfall is running 20% behind demand, compared with 15% at the end of 1987.

Executives at chip makers agree that the shortage is worsening, blaming much of the gap on the industry's slow moves to add wafer-fabrication capacity as markets recovered in 1987 from history's worst chip recession. Also contributing is the timing of the shift from 256-Kbit to 1-Mbit chips. Production of 1-Mbit chips has not gone smoothly: only one maker, Toshiba Corp., is currently turning out more than one million units a month.

"The spot market is driving the business crazy," says industry analyst Andrew Kessler of PaineWebber Inc. in New York. For 256-Kbit parts in particular, he says, the $4.50 going price is almost twice the minimum under fair market values set by the U.S. government in the trade agreement with Japan. What's more, 1-Mbit DRAM models are selling for about three times the $9 U.S.-Japan treaty price.

Kessler says supply should start to catch up with demand in the third quarter as new production lines in Japan get up to speed. Until then, capacity will fall short. The industry is wary, in the U.S., of boom-bust markets and, in Japan, of worsening trade friction.

Suppliers are proceeding carefully. Motorola Inc. has restarted DRAM production after quitting in the bloodbath of the mid-1980s. National Semiconductor Corp. in Santa Clara, Calif., is studying its options. Texas Instruments Inc. is working under a self-imposed ceiling designed to prevent over-involvement in commodity markets in favor of more profitable segments. The chip maker is currently declining new orders for 256-Kbit chips in 1988.

But capacity is being added. TI, which has been making most of its 1-Mbit parts in Japan, will beef up a Dallas plant to get into volume production during the second half. Motorola is racing to add limited-run production at a plant in Mesa, Ariz., and volume work at a factory in East Kilbride, Scotland, that had been shut down. There is also a joint venture with Toshiba Corp. in Japan.

Meanwhile, NEC is preparing to produce 256-Kbit DRAMs at Roseville, Calif., for shipment worldwide, rather than just in the U.S., says Marck—because most of NEC's plants in Japan are already making 1-Mbit parts. And in Irving, Texas, Hitachi Ltd. has resumed construction of a wafer fab. *–J. Robert Lineback*

THE SITUATION WORSENS

Prices have more than doubled for 256-Kbit random-access memories and delivery has stretched to 16 to 20 weeks in the past year for chips bought in the spot and distribution markets. Here's how the situation has worsened.

- **February 1987:** $1.80 with immediate availability
- **September 1987:** $2.70 with 6-to-8-week availability
- **January 1988:** $3.75 with 16-to-20-week availability
- **February 1988:** $4.50 with 16-to-20-week availability

AUTOMOTIVE

INTEL GETS A JUMP ON THE AUTO MULTIPLEX MARKET

DETROIT

As electronics systems proliferate in cars, chips to support multiplexed vehicle-bus schemes are expected to be one of the next big markets for automotive circuit makers, exceeding $100 million annually by the mid-1990s. And by getting out with silicon early, Intel Corp. is hoping to snatch a dominant position.

At this week's SAE'88 show, sponsored in Detroit by the Society of Automotive Engineers, Intel plans to roll out its 82526 automotive-networking integrated circuit. The part is the first IC to implement the high-performance Controller Area Network (CAN) protocol developed by West Germany's Robert Bosch GmbH, with whom Intel is working.

The 82526, built in Intel's 1.5-μm CHMOS-III process, integrates 30,000 transistors and meets the 1-Mbit/s requirement of so-called Class C automotive networks. Class C nets are aimed at critical applications found in powertrain and vehicle-control subsystems, such as brake signals, which require real-time, interrupt-driven performance.

The 82526 works as a peripheral, offloading message-handling tasks from a host microcontroller. Intel says the chip will go on sale by the third quarter of this year.

But widespread use of the 82526 is still far from assured, particularly among cost-sensitive U.S. auto makers because of industry objections to CAN. Those objections center on a perception that slower, and therefore cheaper, Class B networks will accommodate most needs. But Intel says CAN is also

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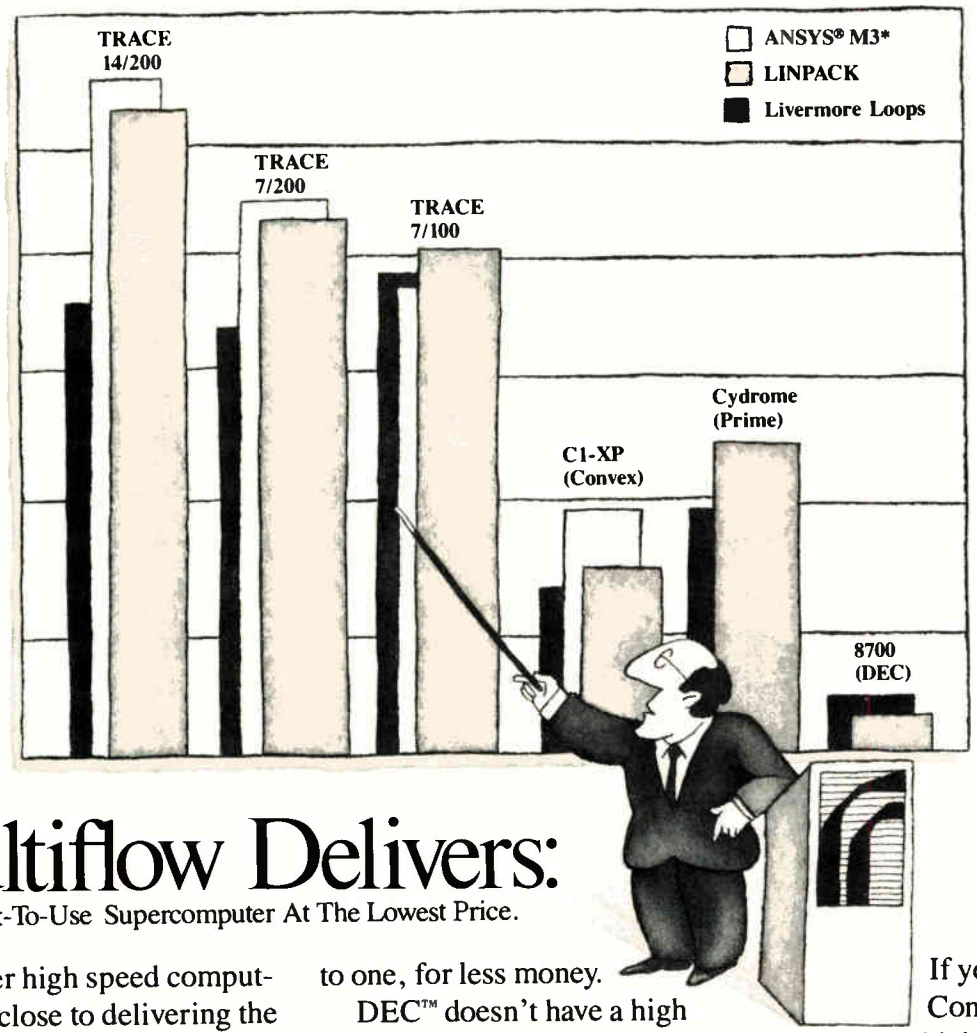

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Radio History

Circle 35 on reader service card

that disk power is necessary in a laptop, they think other features might be equally important. "Drive operating power is a major consideration for original-equipment computer manufacturers making laptop portables," says Dataquest's Devin, but makers of true portables are also going to demand reliability and ruggedness. And Devin and Robert Katzive, vice president at Disk/Trend Inc., Mountain View, Calif., which follows the disk business, agree that the 1-in. size of the low-end 3½-in. drive is a major feature because it allows OEMs to replace a floppy-disk drive with a high-performance Winchester version. But Katzive still feels that one other component of the computers must be improved: the display. "Having an adequate display is the gating factor now," he says. "When laptops were announced, the market responded with a loud ho-hum because of the hard-to-read displays." *–Jonah McLeod*

OPTICAL RECORDING

'DIGITAL PAPER' SLASHES COST OF DATA STORAGE

HERTFORDSHIRE, UK

Mass-data-storage costs could be cut to less than half a cent per Mbyte with a flexible "digital paper" optical recording medium developed in the UK by the electronics division of Imperial Chemical Industries plc. The new material from the Welwyn Garden City, Hertfordshire, division of the petrochemicals giant is based on a 25-μm-thick polyester film. The film is coated with a layer of dye that absorbs infrared light and is topped with a protective coating (see drawing, p. 38).

The material is called digital paper because "our main competition is with paper," says Michael Strelitz, ICI Electronics' marketing manager. "The main applications for the new medium will be in offices striving to become paperless."

It stores data in much the same way that optical disks do, using a laser to burn pits 1 μm in diameter in the dye layer. The pits are less reflective than their unburnt counterparts and thus can be read out using the same laser operated at lower power.

The track pitch is 1.6 μm, bringing the effective-data-packing density to more than 10 Mbytes/sq. in. Data-transfer rates meet Ethernet specifications at up to 10 MHz with a signal-to-noise ratio of better than 55 dB. Supplied on a standard 12-in. tape reel carrying 2,400 feet of 35-mm tape, the digital paper costs less than 0.5 cents per Mbyte. Magnetic

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It's called the B-35 mPowerCell™. A CMOS backup battery that you can handle just like any other component. It is tape mounted for automatic insertion. It can be wave soldered. And, it withstands all normal flux cleaning and board drying procedures.

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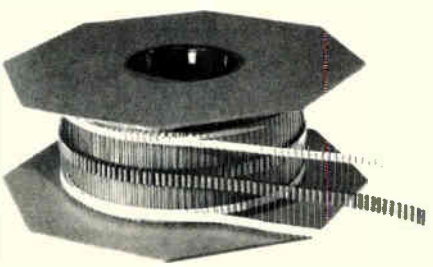
For more information, call (301) 296-7000, ext. 304.



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Electronics

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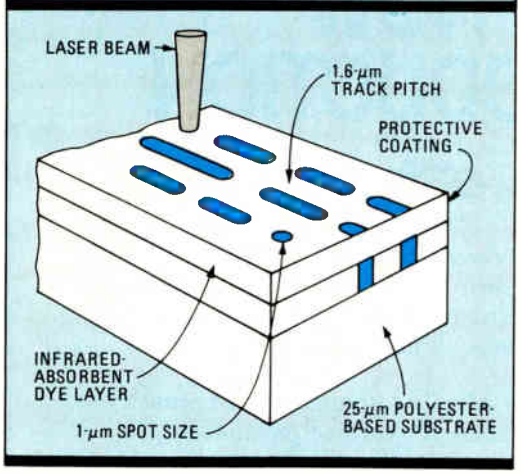
tape in the same format typically costs some 30 times more—around 18 cents per Mbyte, says Strelitz.

ICI Electronics is not content just to make the raw material. It is also determined to break into the end-user market, and plans to sell its digital paper packaged both in computer reels and as 5¼-in. disks. In the latter form, it will be encapsulated in a hard plastic casing with a metal shutter. This will make it physically compatible with the Bernoulli magnetic floppy-disk cartridge produced by Iomega Inc., Roy, Utah. ICI Electronics developed the cartridge with Iomega.

For the tape, ICI collaborated with CREO Electronics Corp. of Burnaby, B. C., Canada. CREO is working on a mass optical-tape drive compatible with the IBM 3400, using ICI's tape. The formatted, error-corrected capacity of the tape for the system will be 1,000 gigabytes. Data transfer rate for the drive will be a sustainable 3.0 Mbytes per second, conforming to IBM mainframe standards. A maximum of 28 seconds will be needed to read any single byte.

The system is being developed under contract to the Canadian government for use in military and civil applications. Typical civilian applications include satellite data acquisition, geophysical and meteorological data archiving, medical imaging, document imaging, and audit trail recording in large data processing installations. *–Peter Fletcher*

DIGITAL PAPER STORES 10 MBYTES/SQUARE INCH



Pits burned by a laser record 0s and 1s in ICI Electronics' digital paper. The pits are read out optically.

TESTERS

E-BEAM TESTER IS FIVE TIMES MORE ACCURATE

MUNICH

A two-year crash design program at Siemens AG has spawned an electron-beam tester that measures voltages on submicron VLSI circuits with an accuracy to within 10%, about five times better than today's e-beam methods. The system, developed at Siemens' Central Research Laboratories in Munich and available commercially, is part of the Siemens-Philips Megaproject, itself a crash program begun in 1984 to serve as a technology locomotive for the high-density, high-complexity VLSI circuits of the 1990s.

Siemens rushed the tester to evaluate those chips. Megaproject's immediate goals are full production next year of a 1-Mbit static random-access memory by Philips and a 4-Mbit dynamic RAM by Siemens, bringing the companies up to par with the Japanese in high-density memories.

The system uses an e-beam probe with

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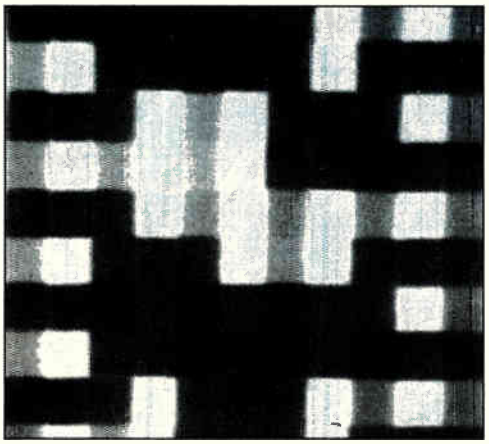
a 0.1-μm spatial resolution at an electron acceleration voltage of 1 kV and a probe current of 2 nA. The tester determines voltages on submicron lines down to 0.5 μm wide. A retarding-field spectrometer integrated into the objective lens ensures that the line-to-line voltage coupling is less than 2% for 1-μm lines.

Typically, Japanese companies are also doing advanced research on e-beam testers. Hitachi Ltd. is developing a system that will match the Siemens machine's spatial resolution and accuracy, says Eckhard Wolfgang, head of the Microelectronics Circuit Analysis Department at the Munich labs. But the German tester is already being sold by Integrated Circuit Testing GmbH—as the 9010—for about $400,000. It can be linked to a computer-aided-design station to form a setup similar to Sentry Schlumberger Inc.'s IDS 5000 [*Electronics*, April 30, 1987, p. 51].

In designing their tester, the Siemens researchers had to find a compromise between acceleration voltage and spatial resolution. Ordinarily, the higher that voltage, the better the resolution. But a high acceleration voltage also can damage the chip.

So the design optimizes the e-beam optics for an acceleration voltage of 700 to 1,500 V, says Wolfgang. That value, which contrasts with 20 to 40 kV for typical scanning electron microscopes, is low enough not to damage the chip.



On the five-line internal bus of a 4-Mbit DRAM, the dark areas represent 1s, and the bright areas 0s.

The high spatial resolution is achieved by keeping the working distance—that is, the magnetic lens-to-chip distance—extremely low, just 2 mm. This puts the 0.1-μm-diameter electron probe smack on submicron lines, with potentials on neighboring lines not influencing the measurement. That explains the tester's high accuracy.

To work at low voltage with the highest possible probe current in a finely focused spot, the tester uses a set of three new electron optical components: an optimized single-crystal lanthanum-hexaboride electron gun, an immersion condenser lens, and a compound spectrometer objective lens.

The long-life electron gun operates at a high extraction voltage, typically 5 kV, and a high extraction field, around 4 kV/mm. This results in a beam brightness, and consequently probe-current density, high enough to free a sufficient number of secondary electrons from the probed lines.

The immersion condenser lens decelerates the electrons from their initial energy of five kiloelectronvolts (keV) to the final energy of between the harmless 700 to 1,500 electronvolts, while at the same time maintaining the gun's high brightness.

The spectrometer objective lens is a low-aberration focusing element designed for use as an electron spectrometer. The secondary electrons generated at the chip are extracted by a high electrostatic field and focused by the lens into a crossover that coincides with the center of the hemispherical grids of the spectrometer. *–John Gosch*

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Wren III H.H.	94	18	SCSI	10
Wren III	160.7	16.5	SCSI	10
Wren III	182	16.5	ESDI	10
Wren II H.H. RLL	65.8	28	ST506	7.5
Wren II H.H.	40.5	28	ST506	5
Wren II RLL	109	28	ST506	7.5
Wren II	75.5	28	ST506, ESDI, SASI	5

H.H. = Half High Models
All models list useable formatted capacity.
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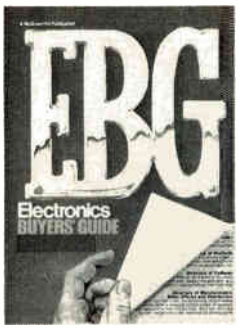

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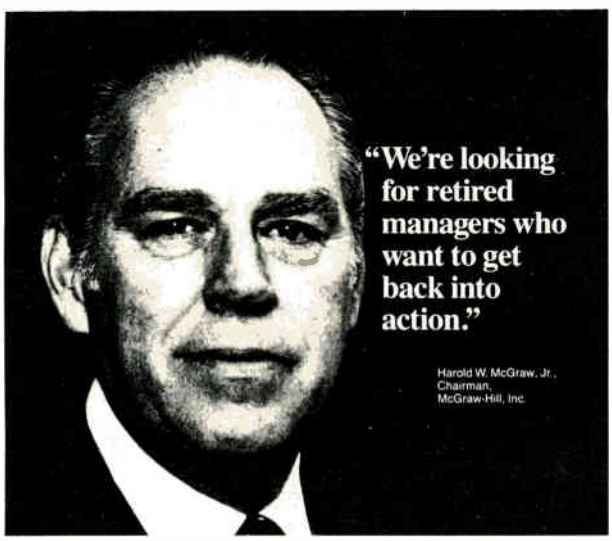

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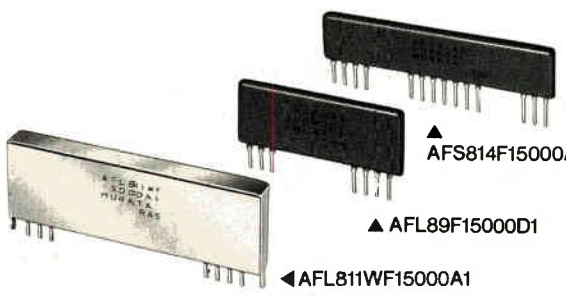

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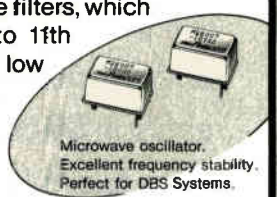

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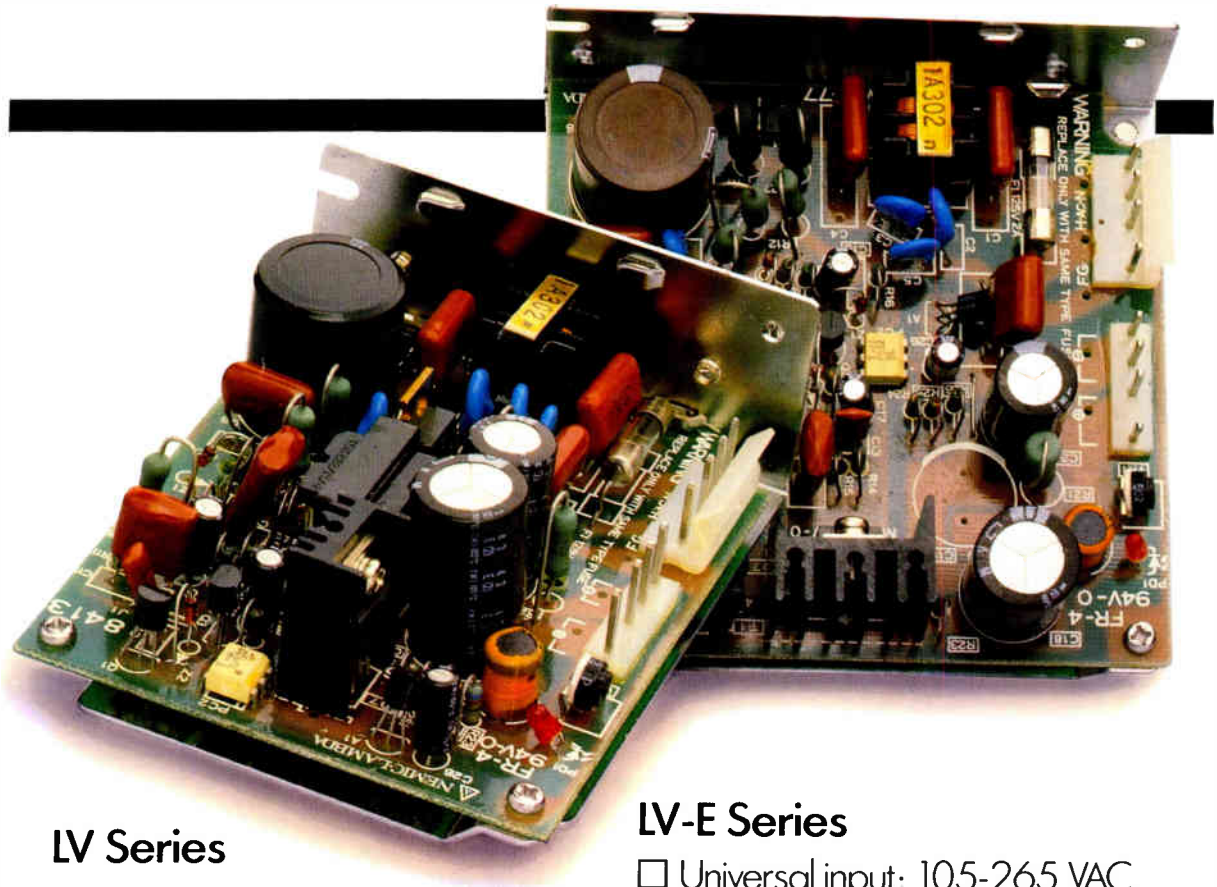

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	3.0	3.0	2.25	35.00	29.75	28.50	27.00	LVS-43-5B
	5.0	5.0	3.75	51.00	39.00	37.25	35.75	LVS-44-5B
	10.0	10.0	7.50	74.00	63.75	52.00	47.50	LVS-45-5B
12V ± 5% ADJ.	0.9	0.9	0.67	28.00	23.75	23.25	22.25	LVS-42-12B
	1.3	1.3	0.97	35.00	29.75	28.50	27.00	LVS-43-12B
	2.1	2.1	1.57	51.00	39.00	37.25	35.75	LVS-44-12B
	4.2	4.2	3.15	74.00	63.75	52.00	47.50	LVS-45-12B
15V ± 5% ADJ.	0.7	0.7	0.52	28.00	23.75	23.25	22.25	LVS-42-15B
	1.0	1.0	0.75	35.00	29.75	28.50	27.00	LVS-43-15B
	1.7	1.7	1.27	57.00	39.00	37.25	35.75	LVS-44-15B
	3.4	3.4	2.55	74.00	63.75	52.00	47.50	LVS-45-15B
24V ± 5% ADJ.	0.5	0.5	0.37	28.00	23.75	23.25	22.25	LVS-42-24B
	0.7	0.7	0.52	35.00	29.75	28.50	27.00	LVS-43-24B
	1.1	1.1	0.82	51.00	39.00	37.25	35.75	LVS-44-24B
	2.1	2.1	1.57	74.00	63.75	52.00	47.50	LVS-45-24B
28V ± 5% ADJ.	0.4	0.4	0.30	28.00	23.75	23.25	22.25	LVS-42-28B
	0.6	0.6	0.45	35.00	29.75	28.50	27.00	LVS-43-28B
	0.9	0.9	0.67	51.00	39.00	37.25	35.75	LVS-44-28B
	1.8	1.8	1.35	74.00	63.75	52.00	47.50	LVS-45-28B
48V ± 5% ADJ.	0.2	0.2	0.15	28.00	23.75	23.25	22.25	LVS-42-48B
	0.3	0.3	0.22	35.00	29.75	28.50	27.00	LVS-43-48B
	0.5	0.5	0.37	51.00	39.00	37.25	35.75	LVS-44-48B
	1.0	1.0	0.75	74.00	63.75	52.00	47.50	LVS-45-48B

LV Series. Triple Output. 120VAC Input.

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	0.3	0.3	0.15					+12	
	0.2	0.2	0.1					−12	
	3.0	1.5	—	91.00	73.00	59.00	53.50	+ 5	LVT-41-133B
	1.2	0.6	—					+12	
	0.3	0.15	—					−12	
5V ± 15V FIXED	2.0	2.0	1.0	62.00	49.50	40.50	36.50	+ 5	LVT-40-144B
	0.3	0.3	0.15					+15	
	0.2	0.2	0.1					−15	
	3.0	1.5	—	91.00	73.00	59.00	53.50	+ 5	LVT-41-144B
	1.2	0.6	—					+15	
	0.3	0.15	—					−15	
5V ± 12V-5V FIXED	2.0	2.0	1.0	62.00	49.50	40.50	36.50	+ 5	LVT-40-131B
	0.3	0.3	0.15					+12	
	0.2	0.2	0.1					− 5	
	3.0	1.5	—	91.00	73.00	59.00	53.50	+ 5	LVT-41-131B
	1.2	0.6	—					+12	
	0.3	0.15	—					− 5	

LV-E Series. Extended Range. Single Output. 105 to 265VAC Input.

	MAX CURRENT (AMPS AT) 40°C	50°C	60°C	PRICE QTY. 1	QTY. 100	QTY. 250	QTY. 1000	MODEL
5V ± 5% ADJ.	2.0	2.0	1.50	$43.00	$38.50	$35.00	$34.00	LVS-42E-5
	3.0	3.0	2.25	51.00	46.00	40.75	38.50	LVS-43E-5
	5.0	5.0	3.75	79.00	71.00	63.25	59.75	LVS-44E-5
	10.0	10.0	7.50	106.00	95.50	85.00	80.50	LVS-45E-5
12V ± 5% ADJ.	0.9	0.9	0.67	43.00	38.50	35.00	34.00	LVS-42E-12
	1.3	1.3	0.97	51.00	46.00	40.75	38.50	LVS-43E-12
	2.1	2.1	1.57	79.00	71.00	63.25	59.75	LVS-44E-12
	4.2	4.2	3.15	106.00	95.50	85.00	80.50	LVS-45E-12
15V ± 5% ADJ.	0.7	0.7	0.52	43.00	38.50	35.00	34.00	LVS-42E-15
	1.0	1.0	0.75	51.00	46.00	40.75	38.50	LVS-43E-15
	1.7	1.7	1.27	79.00	71.00	63.25	59.75	LVS-44E-15
	3.4	3.4	2.55	106.00	95.50	85.00	80.50	LVS-45E-15
24V ± 5% ADJ.	0.5	0.5	0.37	43.00	38.50	35.00	34.00	LVS-42E-24
	0.7	0.7	0.52	51.00	46.00	40.75	38.50	LVS-43E-24
	1.1	1.1	0.83	79.00	71.00	63.25	59.75	LVS-44E-24
	2.1	2.1	1.57	106.00	95.50	85.00	80.50	LVS-45E-24
28V ± 5% ADJ.	0.4	0.4	0.30	43.00	38.50	35.00	34.00	LVS-42E-28
	0.6	0.6	0.45	51.00	46.00	40.75	38.50	LVS-43E-28
	0.9	0.9	0.67	79.00	71.00	63.25	59.75	LVS-44E-28
	1.8	1.8	1.35	106.00	95.50	85.00	80.50	LVS-45E-28
48V ± 5% ADJ.	0.2	0.2	0.15	43.00	38.50	35.00	34.00	LVS-42E-48
	0.3	0.3	0.22	51.00	46.00	40.75	38.50	LVS-43E-48
	0.5	0.5	0.37	79.00	71.00	63.25	59.75	LVS-44E-48
	1.0	1.0	0.75	106.00	95.50	85.00	80.50	LVS-45E-48

LV-E Series. Extended Range. Triple Output. 85 to 265VAC Input (LVT-40E, 41E 105 to 265VAC)

	MAX CURRENT (AMPS AT) 40°C	50°C	60°C	PRICE QTY. 1	QTY. 100	QTY. 250	QTY. 1000	Volt Vo	MODEL
5V ± 12V FIXED	1.00	1.00	0.70	$55.00	$49.00	$40.00	$38.50	+ 5	LVT-38E-133
	0.10	0.10	0.07					+12	
	0.10	0.10	0.07					−12	
	2.00	2.00	1.40	78.00	62.75	51.25	45.75	+ 5	LVT-39E-133
	0.30	0.30	0.21					+12	
	0.20	0.20	0.14					−12	
	2.00	1.80	1.20	71.00	57.00	52.50	48.25	+ 5	LVT-40E-133
	0.30	0.27	0.18					+12	
	0.20	0.18	0.12					−12	
	3.00	2.00	1.30	105.00	84.00	67.75	61.75	+ 5	LVT-41E-133
	1.20	0.80	0.50					+12	
	0.30	0.20	0.13					−12	
	3.00	3.00	2.10	116.00	90.00	70.00	61.75	+ 5	LVT-42E-133
	0.40	0.40	0.28					+12	
	0.40	0.40	0.28					−12	
5V ± 15V FIXED	1.00	1.00	0.70	55.00	49.00	40.00	38.50	+ 5	LVT-38E-144
	0.10	0.10	0.07					−15	
	0.10	0.10	0.07					−15	
	2.00	2.00	1.40	78.00	62.75	51.25	45.75	+ 5	LVT-39E-144
	0.30	0.30	0.21					+15	
	0.20	0.20	0.14					−15	
	2.00	1.80	1.20	71.00	57.00	52.50	48.25	+ 5	LVT-40E-144
	0.30	0.27	0.18					+15	
	0.20	0.18	0.12					−15	
	3.00	2.00	1.30	105.00	84.00	67.75	61.75	+ 5	LVT-41E-144
	1.20	0.80	0.50					+15	
	0.30	0.20	0.13					−15	
	3.00	3.00	2.10	116.00	90.00	70.00	61.75	+ 5	LVT-42E-144
	0.40	0.40	0.28					+15	
	0.40	0.40	0.28					−15	

World Radio History

LV, LV-E SERIES Specifications

DC OUTPUT
Voltage range shown in tables.

REGULATED VOLTAGE

regulation, line ..... 0.4% for input variations from 85 to 132VAC or 132 to 85VAC on all LV models. 0.4% for input variations from 105 to 265VAC or 265 to 105VAC on LVS-E, LVT-40E, 41E models. (LVS-45E models: 0.4% for input variations from 95 to 132VAC or 132 to 95VAC when wired for 110V operation; 187 to 265VAC or 265 to 187VAC when wired for 220V operation.) 1.0% for input variations from 85 to 265VAC or 265 to 85VAC on LVT-38E, 39E, 42E models.

regulation, load ..... 0.8% for LVS, LVS-E and LVT-40E, 41E models. 2% for LVT: LVT-38E, 39E, 42E models (from no load to full load and full load to no load)

ripple and noise ..... 15mV RMS for all models with either positive or negative terminal grounded. 150mV pk-pk for 5V models; 300mV pk-pk for 12V through 48V models and second and third outputs of LVT models.

temperature coefficient ..... 0.02%/°C for LVS, LVS-E, LVT-40E, 41E models and 5V output of LVT models. 0.03%/°C for other two outputs of LVT models and for main output of LVT-38E, 39E, 42E, 0.05%/°C on other two outputs of these models.

AC INPUT
85 to 132VAC, 47-440Hz on all LV models. 105 to 265VAC, 47-440Hz on LVS-E and LVT-40E, 41E models. The LVS-45E is jumper selectable for 95 to 132VAC or 187 to 265VAC operation (factory pre-wired for 220V operation). 85 to 265VAC, 47-440Hz on all LVT-38E, 39E, 42E models.

DC INPUT
110 to 175VDC for LV models. 145 to 370VDC for LVS-E and LVT-40E, 41E. LVS-45E allows DC input (260 to 370VDC) only, when used for 220VAC operation. 110 to 330VDC for LVT-38E, 39E, 42E.

EFFICIENCY
62% minimum on all LVS, LVT, LVT-40E, 41E and LVS-E models. 64% typical on LVT-38E, 39E, 42E models.

OVERSHOOT
No overshoot at turn-on, turn-off or power failure.

AMBIENT OPERATING TEMPERATURE
0-60°C with suitable derating above 50°C. LVT-40E and 41E derate above 40°C. 0-50°C for LVT-41. (See Tables.)

STORAGE TEMPERATURE RANGE
−30°C to +85°C.

OVERLOAD PROTECTION
Automatic electronic current limiting circuit with automatic recovery, limits short circuit output current to a safe, preset value, thereby protecting the load as well as the power supply when direct shorts occur. Sustained short circuit operation for more than 30 seconds may cause damage to the power supply.

HOLD UP TIME
Output will remain within regulation limits for 16 msec typical for all models (20 msec typical at 100VAC for LVT-38E, 39E, 42E models) after loss of AC power at full load with nominal output voltage and 85VAC input at 60Hz (110V RMS, 60Hz on LVS-E models). On LVS-45E this is true at 105V RMS when wired for 110V operation, or 210V RMS when wired for 220V operation.

OVERVOLTAGE PROTECTION
Standard on all single output LVS-44, LVS-45, LVS-44E, LVS-45E and on main output of LVT-38E, 39E, 42E models.

COOLING
Convection cooled, no fans or blowers needed.

INPUT FUSE
A 2 amp slo-blo fuse in the AC input line protects the input wiring to the power supply. Overload of power supply does not cause fuse failure.

DC OUTPUT CONTROLS
Simple screwdriver adjustment over the entire voltage range of single output models. Triple output models are fixed.

OUTPUT STATUS INDICATOR
LED indicates presence of voltage on single output models and on +5V output of triple models.

INPUT AND OUTPUT CONNECTIONS
Molex connectors. AC input—Molex Type 5289-4A. DC output—Molex Type 5287-4A. (Molex Type 5287-5A on triples). AC input terminals are marked "H" and "N" for hot side and neutral respectively. LVT-38E, 39E, 42E use Amp 171141-1 for AC input and Amp 171216-1 for DC outputs.

MOUNTING
Two mounting surfaces, three mounting positions. Air circulation may be required when mounting in confined areas. Two mounting positions on LVT-38E, 39E, 42E.

PHYSICAL DATA

Package Model	Lbs. Net	Lbs. Ship	Size Inches
LVS-42, 42E	0.44	0.52	1.38 × 3.82 × 3.13
LVS-43, 43E	0.55	0.64	1.38 × 3.82 × 3.88
LVS-44, 44E	0.70	0.82	1.38 × 3.82 × 4.59
LVS-45, 45E	0.86	1.00	1.46 × 3.82 × 6.26
LVT-38E	0.35	0.42	1.38 × 1.97 × 4.33
LVT-39E	0.44	0.52	1.57 × 2.36 × 4.33
LVT-40, 40E	0.84	1.00	1.38 × 3.82 × 4.47
LVT-41, 41E	1.00	1.13	1.46 × 3.82 × 6.05
LVT-42E	0.66	0.75	1.57 × 2.36 × 5.91

FINISH
Plated steel chassis.

GUARANTEE
90-day guarantee includes labor as well as parts. Guarantee applies to operation at full published specifications at end of 90 days.

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VDE
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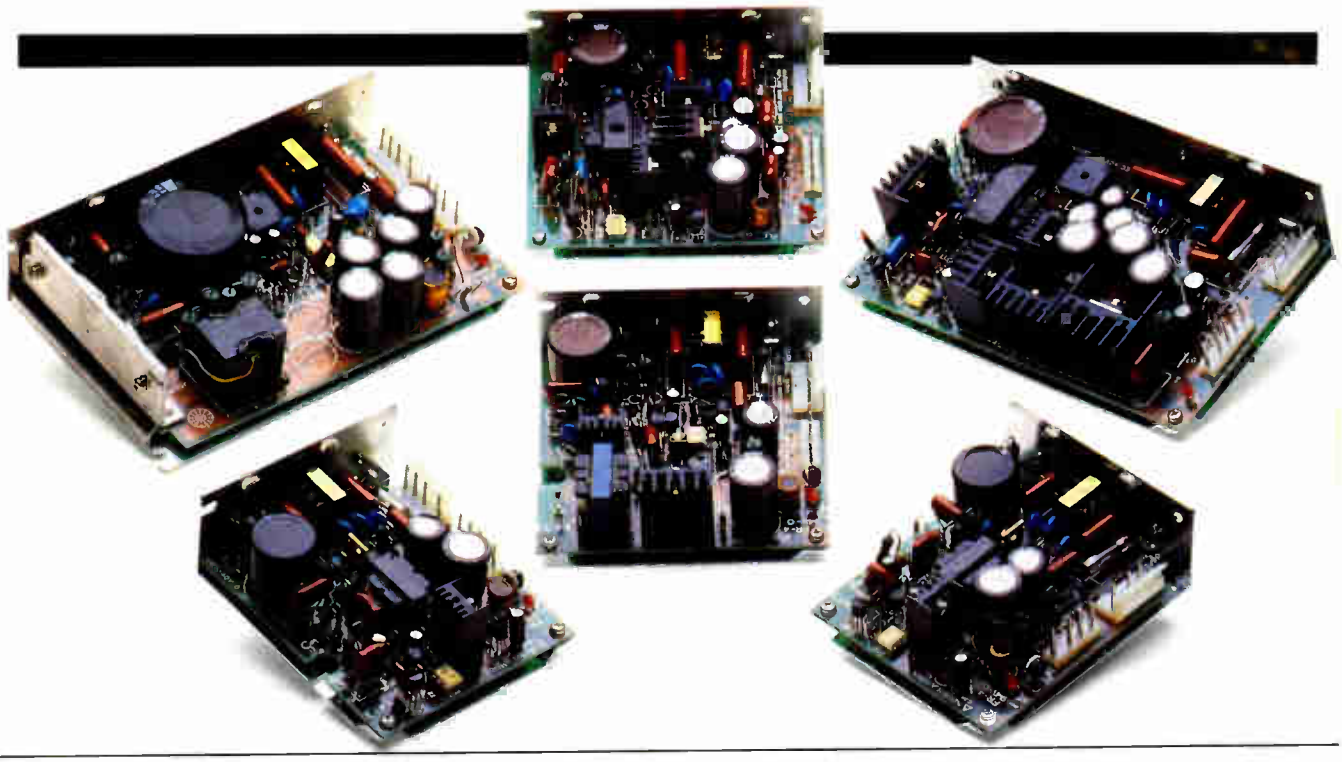

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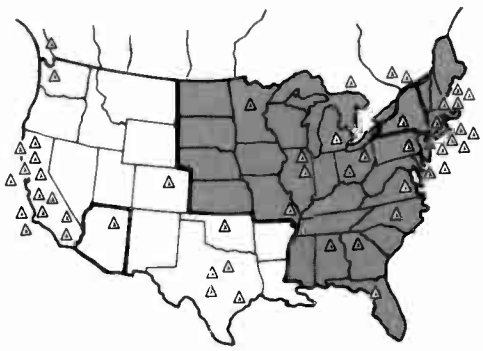

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PROBING THE NEWS

HIGH-DENSITY FLASH EEPROMS ARE ABOUT TO BURST ON THE MEMORY MARKET

They could end up being the dominant low-cost, high-density memory

by J. Robert Lineback

The market is about to be hit with a wave of new electrically erasable nonvolatile memory chips that may soon match the bit density of dynamic random-access memories. This emerging breed of programmable read-only memories—built with single-transistor cells and called flash EEPROMs—could pack 64 Mbits on a chip by the turn of the century.

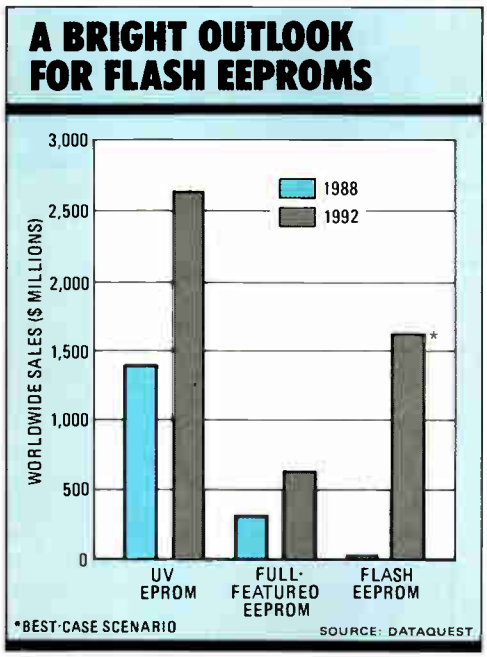
At least a half dozen silicon merchants—among them such giants as Intel, National Semiconductor, Texas Instruments, and Toshiba—are working on flash EEPROMs, using a variety of cell layouts (see figure). First out of the gate will be a CMOS 512-Kbit flash EEPROM, coming this month from Seeq Technology Inc. in San Jose, Calif. Right on Seeq's heels is Intel Corp., which has developed what executives will only say is a significant "process trick" for its flash parts that allows it to use the same design as in its ultraviolet erasable PROMs.

RADICAL CHANGE. Intel believes that by the year 2000, flash memories will emerge as the low-cost, high-density champion memory. If they are right, flash EEPROMs could radically change system architectures, making it possible to build computers with all-solid-state memory systems. The flash EEPROMs would be the only direct-access mass storage in the system, replacing disk drives feeding DRAM-based main memory.

Flash memories are a marriage of conventional EEPROM and EPROM technologies, offering the high densities of EPROM thanks to one-transistor cells. The write operation is like that of EPROMs, using hot-electron injection. The erase operation borrows the mechanism of floating-gate EEPROMs—electrical erasure by cold-electron tunneling.

Most full-featured EEPROMs have two-transistor cells and can reprogram individual bytes one at a time. In contrast, the entire contents of flash-EEPROM arrays are erased quickly and simultaneously. The flash memory trades selective-erase capabilities for space-saving single-transistor cells.

"Flash" also describes the way the new memory's market segment is expected to grow, surging from near nothing today to over $1 billion in the early 1990s (see chart, left). The flash movement has become so explosive that market researcher Dataquest Inc., San Jose, Calif., is waiting for key product unveilings before it will venture any formal forecasts of the business's growth. "We have made some initial estimates that show it could represent a third of the total nonvolatile area [by 1992], if all of the companies we think are going to be in the business are actually in volume production," says Mary Olsson, an industry analyst at Dataquest.



The potential density of EEPROMs is what has got everyone excited. DRAMs are hitting a density barrier, says Bruce McCormick, product marketing manager at Intel—it is getting harder and harder to reduce the space needed for the capacitors that store charge in each cell to retain data. Many flash-memory proponents agree. They see nothing but problems for DRAM makers trying to push the density of their parts in coming years.

Most observers also agree, though, that flash parts will not threaten DRAMs right away. Nor will they cut quickly into EEPROM sales. Right now they pose a real threat to EPROMs. Because of their high cost, conventional EEPROMs did not, as some thought they would, push EPROMs out of the market. Flash EEPROMs, however, could succeed where full featured EEPROMs failed.

Although flash has tremendous market potential, vendors are being cautious about projections. "There will be room for all three types of nonvolatile memory: flash, UV-EPROM, and full-featured EEPROM," says Mike Vilott, vice president of marketing at Seeq. "There is a slight price and space penalty for flash, but there are also benefits." The benefits are electrical erasability and the ability to test parts, which can not be done for EPROMs in cheap windowless packages.

Two styles of flash memories are being developed by most suppliers. One is aimed at EPROM sockets, the other at price-sensitive EEPROM jobs that don't require byte erasure. Seeq is working on products in both styles.

Seeq, the first company to move flash EEPROMs into the marketplace with an nMOS part [*Electronics*, Aug. 21, 1986, p. 53], uses a split-gate layout. The top layer of polysilicon forms the control gate, slopping down over a portion of the channel to form a select device. The folded-structure cell takes up about 10% more space than a conventional EPROM cell, says Gary Rauh, strategic marketing manager at Seeq, which will use its split-gate design in the CMOS flash memories being introduced later this month.

Allied with Seeq and also working on the design of the two flash families is National Semiconductor Corp. The pact between Seeq and National, signed last fall, is aimed at establishing feature-set standards quickly in the emerging market. They need to move fast; coming up behind them are a host of major semiconductor merchants, notably Intel.

Managers at Intel won't say much

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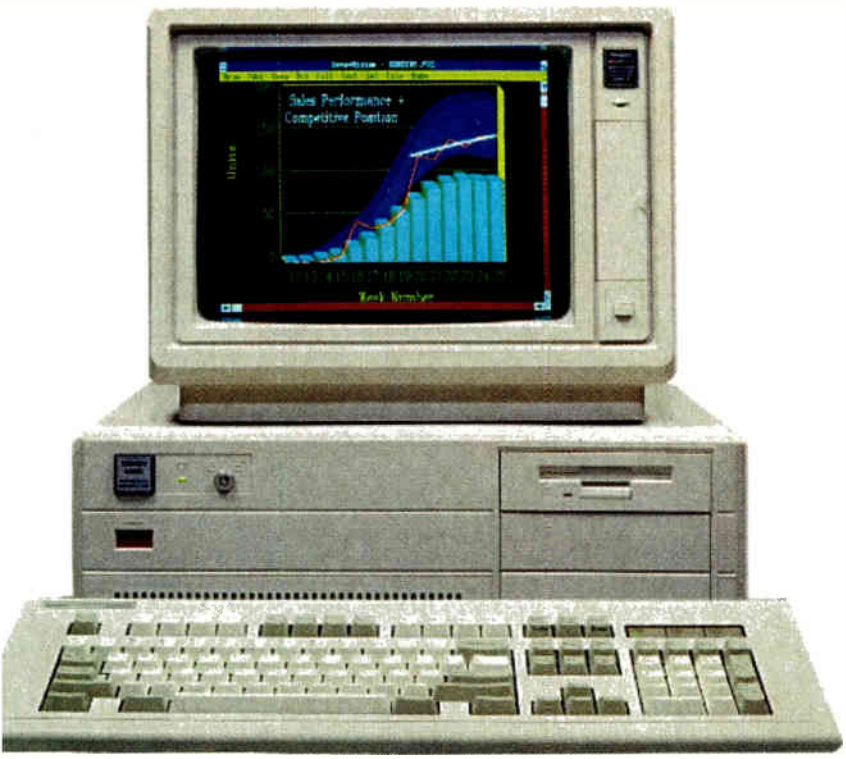

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SPECIAL ISSUE

SUPERCOMPUTERS: THE PROLIFERATION BEGINS

Now the hottest computer game around, growing at nearly 40% annually, they include a rapidly widening collection of products, large and small; with the current flood of introductions, they range from the traditional monsters to single-user 'desktop' models

by Tom Manuel

Supercomputers are proliferating all up and down the price and performance spectrum, in essence redefining the nature of supercomputing. The field now spans a range from single-user systems that may deliver nearly the full power of the first modern supercomputer, the Cray-1, to machines with almost 25 times the Cray-1's power. New circuit technology, as well as advances in hardware and software architecture, is driving prices down, making it easier for those who want a supercomputer to buy one. For under $1 million, users can buy a machine with the same performance of the previous generation's largest supercomputer. So the installed base is exploding as potential users realize that the number-crunching function of supercomputers can be applied beyond scientific and military applications: to product design, business, and much more.

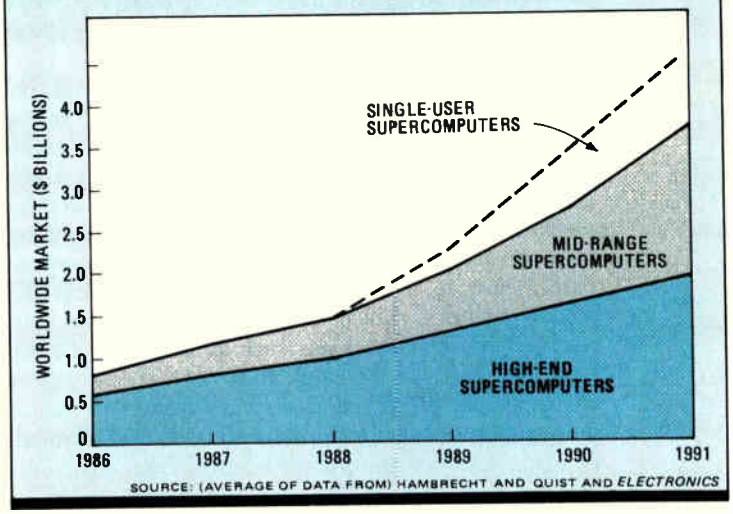
And the number of supercomputer suppliers is exploding, as well. The pace of new product introductions has been furious in 1988's first quarter. Four are introduced in this special issue alone. At least five other introductions were unveiled in recent weeks, and several more are expected soon. That would mean adding more companies to the 31 vendors that currently have supercomputer products (see table, p. 53). And applications are taking off as software, much of it based on the burgeoning number of parallel-processing architectures, becomes available (see p. 75).

But as good as the news is, some analysts are cautioning that there are so many companies scrambling in the minisupercomputer and midrange market that a shakeout may occur. It could even be under way. The spectre of Japanese competition in the world market also hangs over the U.S. supercomputer industry. Although a trend to parallel architectures is clear in the U.S., the Japanese are sticking to single-processor technology (see p. 57). In the U.S., the Japanese have not jumped the hurdles necessary to make inroads and even on their home turf, Cray Research Inc. of Minneapolis still holds its commanding position.

Japan is not the only threat to the supercomputer market's upstarts, however. Everyone is waiting to see what the two largest U.S. computer companies, IBM Corp. and Digital Equipment Corp. (see p. 56), are going to do in supercomputers. How the marketing pie is eventually divided will depend on many factors, including how the spate of available technologies and systems eventually match up to application areas.

One way to look at the computer spectrum is as a triangle with three layers, says Steven Chen, founder and president of Supercomputer Systems Inc., Eau Claire, Wis. (see p. 54). Supercomputers are at the apex, mainframes in the middle, and work stations—the broadest market and most competitive—at the bottom. "Historically, as supercomputer vendors have extended

NEW TYPES SHOULD FUEL GROWTH



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JAPAN FOCUSES ON SIMPLE BUT FAST SINGLE-PROCESSOR SUPERCOMPUTERS

Not yet following the U. S. into multiprocessor designs, Japan relies on its device-level strengths to build powerful systems; but it lacks a broad selection of commercial software for them

by Charles L. Cohen

The Japanese take the old-fashioned approach to supercomputer architecture. "Supercomputers should be simple, like Japanese haiku," says one Japanese expert. Although their big machines are not as simple as their classical 17-syllable poems, the Japanese do avoid complex multiprocessor architectures.

So while U. S. supercomputer makers charge off into a wild array of new multiprocessor approaches, the Japanese stick to simpler single-processor architectures. And their supercomputers are the speediest one-processor machines in the world—by far—thanks primarily to advanced semiconductor technology. The only way U. S. supercomputers can come near their processing rates is in multiprocessor configurations.

But the Japanese may eventually have to fall back on multiprocessor systems to stay in the horsepower race. In fact, the supercomputer that Fujitsu Ltd. is building for a government-sponsored research project will have multiple processors. But this is strictly a research vehicle, and Japanese vendors so far are resisting the move for commercial systems.

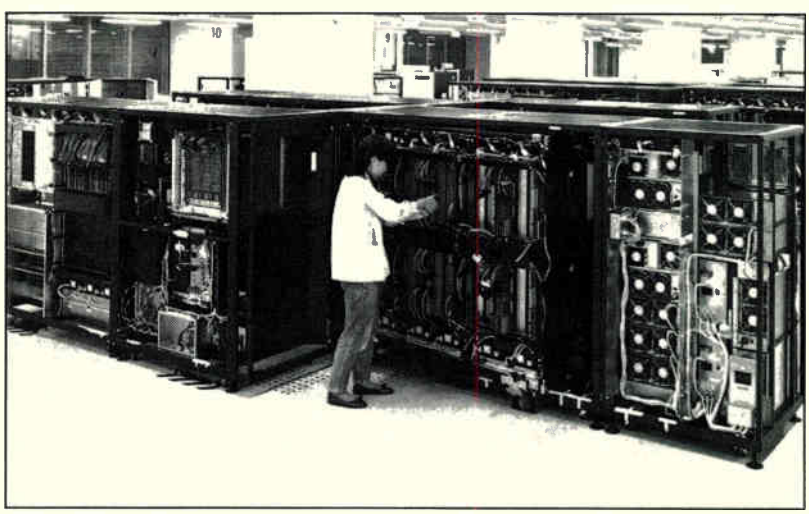
Another difference between Japan and the U. S. is that Japan has no real midrange or low-end supercomputers. The Japanese strength is mostly in building machines like those from Cray Research Inc.—huge, price-no-object number crunchers that push the performance limits of technology.

The biggest problem Japanese supercomputer makers face is in software. Although their systems are fast, there is relatively little application software ready to run on them. Users with their own Fortran programs can step up to a Japanese machine and get them working with an excellent autovectorizing compiler (see p. 58), but a wide variety of commercial-grade third-party software is not available. Neither of the two major trends in the U. S. supercomputer software industry—the moves to parallel programming and the Unix operating system (see p. 76)—is visible in Japanese product announcements.

Most Japanese supercomputers have evolved from mainframe products. The supercomputers have vector- or array-processing hardware attached, as well as other modifications to boost performance.

The fastest of them is built by Hitachi Ltd., Tokyo, whose top-end S-820 boasts a peak execution rate of 3 billion floating-point operations/s. It is based on the company's M-680H mainframe, to which vector registers and other hardware have been added. The company's prowess in semiconductor technology, especially high-speed memory chips, gets most of the credit for the machine's performance, says Raul Mendez, the Colombian-born director of the Institute for Supercomputing Research, Tokyo. The S-820 even beats out multiprocessor supercomputers like the 1.2-gigaflops X-MP from Cray. The Cray Y-MP, due in the third quarter, will pull ahead again, says the Minneapolis company, but only with eight processors working together.

The VP-series supercomputers from Fujitsu Ltd., Tokyo (see photo, below), top out at 1.7 gigaflops. They are based on the company's M-380F mainframes. NEC Corp., Tokyo, is the one Japanese player whose supercomputers are not based directly on its mainframe systems. Its 1.3-gigaflops top-of-the-line SX-2A supercomputer consists of two tightly coupled front-end control processors and an array processor. The array processor used in NEC's machines has an original reduced-instruction-set computer architecture,



Fujitsu's VP series supercomputers are tested at the company's Numazu complex; the series tops out at a peak rate of 1.7 gigaflops and is based on its M-380F mainframes.

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CONVEX UNWRAPS ITS FIRST GROWN-UP SUPERCOMPUTER

A 200-Mflops supercomputer that is air-cooled and costs about $1 million propels a new family of products into the supercomputer big time

by Tom Manuel

Convex Computer Corp.'s new supercomputer family is even more of an industry blockbuster than its first system. At a tenfold jump in performance, it's far from just an incremental upgrade over its first minisupercomputer, the C-1. The heart of the new family, the new C-2 processor, churning at 50 million floating-point operations/s, spawns a group of systems whose performance could pass for some fancy supercomputers—namely those of the Cray Research Inc. family.

When added to the C-1, Convex's five new supercomputers create the C series, a six-member product group offering a performance range from 20 to 200 Mflops. They mark an important transition for Convex from a one-product high-tech startup to a multinational company with a wide-ranging product line. It's a tough transition but the Richardson, Texas, company seems to be doing it. (see story, p. 62).

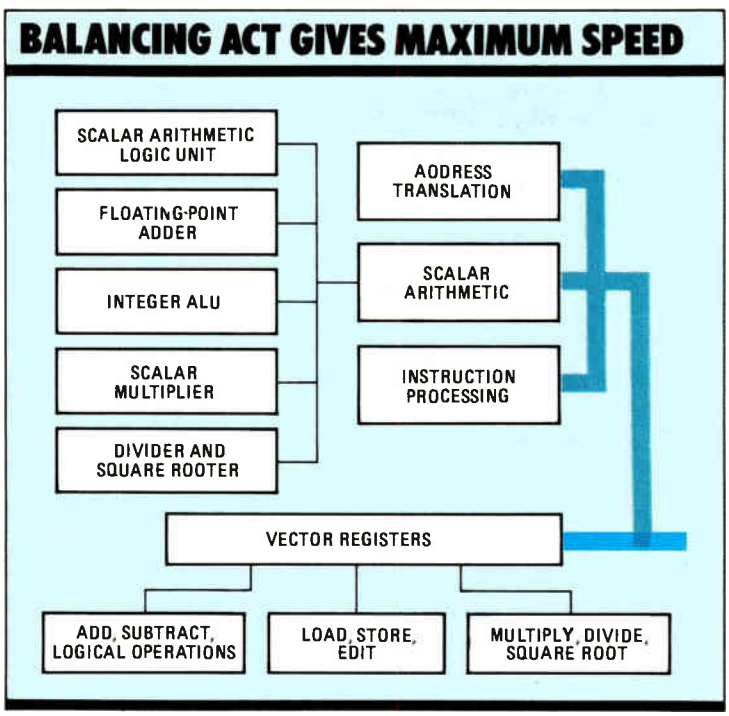
The extended product line propels Convex into the upper end of the minisupercomputer class and nudges it into the low end of the big supercomputers. It positions Convex in an uncrowded segment of the market in the $500,000 to $1 million range offering 50 to 200 Mflops of performance. The company is making this move becuase the minisuper area, which it pioneered, quickly became crowded with new vendors, causing prices and gross margins to drop drastically.

Although of a new design, the new systems are completely compatible with the air-cooled, low-cost vector processing C-1 supercomputer, which startled the industry when it appeared in March 1985. The C series lineup now includes the C120—the new name for the original C-1 machine, the C130, a new midrange machine combining the C-1's architecture with the C-2 central processing unit, and four other new models. These models—the C210, C220, C230, and C240—use between one and four C-2 processors, each of which obtains 50-Mflops capability from employing advanced CMOS and emitter-coupled-logic gate arrays.

The C-2 processor (see fig. 1) balances high-level scalar computation with very fast vector processing. This speeds up throughput because typical job mixes have significant amounts of scalar work to do along with those parts that can be vectorized. In addition, the cycle time is down to 40 ns—from 100 ns on the C-1 machine. But the C-2 processor is not the only major technical innovation by Convex's engineers that move the air-cooled C series into the realm of true supercomputer performance. Three other design enhancements supercharge the systems.

First, a memory system that also relies on ECL circuitry for fast crossbar switching achieves a 200-Mbyte/s bandwidth on each memory port, yielding a total memory-to-processor bandwidth of 800 Mbytes/s in a four-processor system. Second, a new compiler system identifies parallel parts of programs, parts that can be vectorized, and alternative ways to optimize the code. Finally, Convex designers achieved a breakthrough in scheduling tasks for multiprocessing and parallel processing called the automatic self-allocating processor scheme. ASAP delivers the most efficent use of multiple processors running a mixture of jobs of any parallel-processing scheduling scheme available, the company claims.

"The idea was to build the fastest single processor



1. The Convex C-2 processor blends CMOS and ECL VLSI circuits to put both a vector processor and a fast new scalar processor on one board.

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increases the number of jobs completed per unit time—the throughput of the system. Computing with multiple proessors is called parallel processing when more than one processor is used to run different parts of the same program. Parallel processing runs single jobs faster than serial processing. The C series' ASAP scheduling feature runs both multiprocessing and parallel processing at the same time, dynamically and automatically allocating processors to jobs when parallel parts of programs or multiprocessing jobs demand processing time.

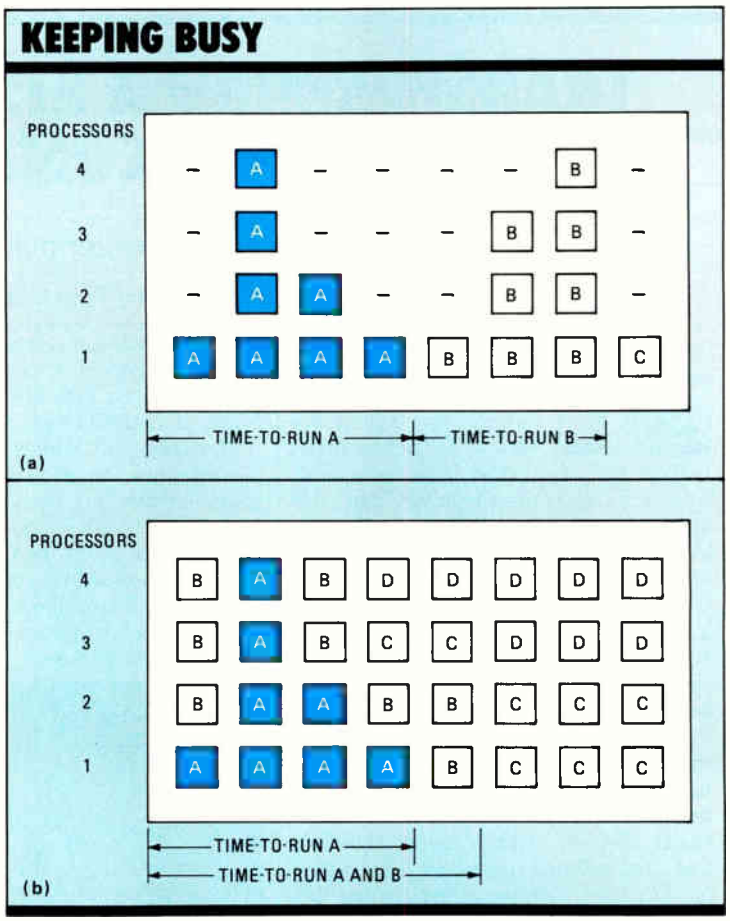
Traditional parallel processing is done with static allocation of processors, in which processors are allocated to one parallel program at a time. When that program is finished, the processors are allocated to the next parallel program. The problem with this approach is that almost no real program is so parallel that it can keep the whole set of processors busy all the time—there are almost inevitably program parts that cannot run in parallel and cannot use more than one processor or parts that can run in parallel but do not use all available processors (see fig. 3a) This form of scheduling wastes processing cycles since, for quite a bit of the time, several processors are idle.

On the other hand, in Convex's ASAP scheme (see fig. 3b) processors are either ready to run or executing code. As soon as a processor has finished a task, it goes to the communications registers looking for work. Work will be waiting in the form of job requests posted in the registers by other processors. As long as there are pending job request flags in the registers, processors keep executing code and are never kept idle when there is something to run. This scheduling method works equally well for multiprocessing, parallel processing, and any mixture of both.

For automatic self-allocating processors to work, the identification, allocation, and implementation of job requests must be fast or the time it takes to schedule tasks will outweigh the benefit of having dynamic scheduling in the first place. To assure low-scheduling overhead, the C-2 designers implemented the mechanisms for automatic self-allocating processors in fast hardware.

On another front, software engineers added parallel processing capability to both the Convex machine's Unix operating system and the vectorizing compiler system. In addition, they added semaphores, which are signals used by processors to post requests and pick up jobs, to the operating system and moved the detailed job and processor scheduling into hardware. The operating system now just does the gross scheduling and the hardware handles the detailed job and processor scheduling. This scheme allows the system to take advantage of fine-grained parallelism that the compiler detects in programs.

The smart and efficient Convex compiler system was enhanced with more optimization techniques and an automatic parallelizing feature. Because the new systems are binary-compatible with the C-1, users do not have to recompile to gain the general speedup of the faster systems. However, users can gain the added advantage of parallel processing from the machine's architecture and the additional optimization techniques by merely recompiling their codes with the new compiler.



3. Static allocation of parallel processors (a) wastes computer cycles. Convex's ASAP scheme (b) keeps all processors busy.

The dynamic code generation added by software engineers then maximizes parallel and vector features. For example, if the number of loop iterations in a program is going to be small, then it generally will not pay to vectorize or parallelize the code in that loop. However, for more iterations, vectorizing the code may yield a net performance improvement, while for even a larger number—over 1,000— of iterations it may pay off to generate parallel processing code and maybe even vectorize it as well.

But the number of iterations may not be known at compile time and it may vary throughout the program's run time. Dynamic code generation will compile for all three cases and at run time, the software checks the number of iterations and branches to the code's optimum version. For example, in the Fortran DO loop statement DO I=1,N; for N less than four, generate scalar code; for N up to 100, (if the code is vectorizable) generate vector code; (if the code is not vectorizable) generate parallel code; and finally, if N is greater than 1,000 (and the loop is vectorizable), generate both vector and parallel code. □

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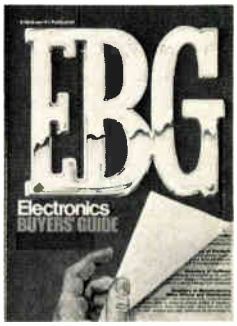

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ARDENT LAUNCHES FIRST 'SUPERCOMPUTER ON A DESK'

The single-user Titan provides the performance of first-generation minisupers for only $150,000; for high-performance graphics work, it has a large vector register file and a graphics processor working hand in hand with its vector and integer processors

by Jonah McLeod

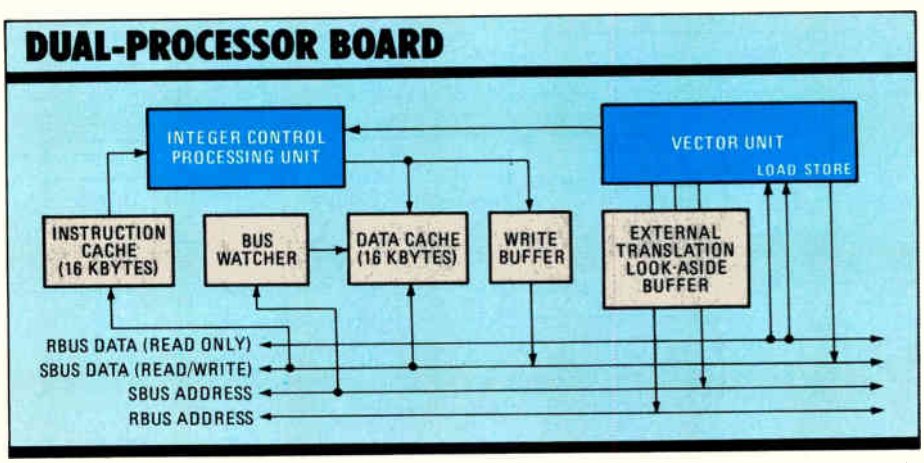
The first of a new breed of supercomputer is now in the marketplace. Ardent Computer Corp. is shipping pre-production models of what it calls a "supercomputer on a desktop." The single-user, graphics-oriented Titan from the Sunnyvale, Calif., startup offers peak performance of 64 million floating-point operations/s and runs the 100-by-100 compiled Linpack benchmark programs at 6 megaflops. That's roughly twice the performance of the first generation of minisupercomputers—but the Titan price peaks at $150,000, where first-generation minisupers run from $500,000 to $1 million.

The Titan gets its cost-effective punch from three features. First, the system contains a proprietary vector processor with a very large vector register file that helps speed up operation. Second, Titan combines its proprietary pixel and polygon processor, which itself offers supercomputer performance, with its vector and integer processors to provide high-performance, high-resolution graphics capability. The Titan boasts a clip-and-perspective divide rate of 200,000 Gourad-shaded triangles/s and a Gourad-shading rate of 50 million pixels/s—performance as good as any current graphics subsystem. Finally, the Ardent system has an optimizing compiler that automatically and efficiently converts applications programs into instructions to run on the vector or the integer processor. This further improves speed; optimizing compilers can double the speed at which a program executes. Ardent also has devised a powerful graphics tool kit that helps users add visual presentations to the results of computing [*Electronics*, Feb. 4, 1988, p. 69]. The whole system fits into a cabinet with a 2-ft. base, standing 4 ft. high.

The Titan also breaks ground in its emphasis on graphics processing. Until now, the engine needed to drive large, computation-intensive simulations has been a room-sized supercomputer that costs over $1 million and requires special wiring and air conditioning. The Titan uses forced air cooling, rather than the elaborate liquid-cooling scheme of fullblown supercomputers, because it makes heavy use of CMOS circuitry. Furthermore, in other supercomputers, the graphics terminal is an add-on that must commmunicate with the processor over a relatively slow data link. Titan's built-in full-color graphics subsystem has high-speed access to the memory and data bus, which gives real-time interactivity with the processor. It can draw 600,000 three-dimensional vectors/s and display them on a 19-in. 1,280-by-1,024-pixel color screen.

The Titan computer was designed by a team attracted to Ardent by Allen Michels and his cofounders (see p. 68). "It is the first of the graphics supercomputers," says Steve Blank, vice president of product marketing. Inside the system cabinet are up to four processor boards and four memory boards providing between 8 and 128 Mbytes of main memory. Titan operates with the industry-standard Unix operating system. The computer, which is currently being shipped to early customers, costs between $79,000 for a single-processor system and $150,000 for a four-processor system.

"The architecture in Ardent's new Titan computer is patterned after the Cray X-MP," says Gordon Bell, Ardent's vice president of engineering and research and development. As with the Cray, Titan has up to four processor boards each with a vector and integer



1. Each Titan processor board holds two processors: the integer processor is a 32-bit RISC chip from MIPS Computer Systems, and the vector processor uses the Weitek floating-point chip set.

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processor (see fig. 1). The integer processors are off-the-shelf 32-bit reduced-instruction-set-computer microprocessors from MIPS Computer Systems Inc. of Sunnyvale, Calif. Ardent is basing its vector processor on the WTL 2264/5 floating-point chip set from Weitek Corp., Sunnyvale, Calif.

What makes the Ardent configuration stand out is its proprietary vector processor and split-bus architecture. "Our vector processor contains a vector register file with more registers than any other architecture," says William Worley, vice president and chief scientist. Vector register files boost the speed of execution and facilitate the operation of the multitasking, multiuser Unix operating system. The Titan vector register file holds 8,000, 64-bit double-precision floating-point numbers.

Also, Titan's architecture provides extensive capability to overlap operations within the vector processor—as much as 30% more than in any supercomputer design to date, says Glen Miranker, chief architect at Ardent. The greater the overlapping in a machine, the greater the parallel execution of vector instructions, he says.

One way the register file boosts execution speed is to store more temporary data in registers. Instructions execute much faster with data in registers before computation than when loading the variables into registers from memory. "As a minimum, there is a 2 to 1 reduction [using a big register file] in the number of memory accesses for a program," says Miranker.

The Titan's vector register file also can address individual elements within a vector. "Titan can perform operations between elements in the vector register file," says Worley. "And it can start and end a vector operation at any segment in the vector." Most other architectures can only address the first element of a vector, and that makes for slower performance of recurrences and other calculations, such as convolutions. The Titan's register file is also dynamically reconfigurable, so the variables for several tasks can be maintained in the file at the same time. Fixed register files can't do that, so they're slower at multiprocessing: they must keep switching the tasks' variables in and out from main memory.

In addition to incorporating the large, flexible register file, the vector processor makes heavy use of pipelining. The processors has five elements, which can be run in parallel: adder, multiplier, and divider, plus two load pipes (ports) to memory, and a store pipe to memory. All five elements can execute instructions simultaneously if the operation of one is not dependent on the outcome of another.

During an addition of vector registers 1 and 2, a dependency exists if the next instruction after the addition is to store the result in vector register 3. Yet another dependency exists if the next following instruction is to load vector register 1 with a new value. If all three instructions occur simultaneously, the second could attempt to store the result before the addition is completed and the third could overwrite a register being used by the first.

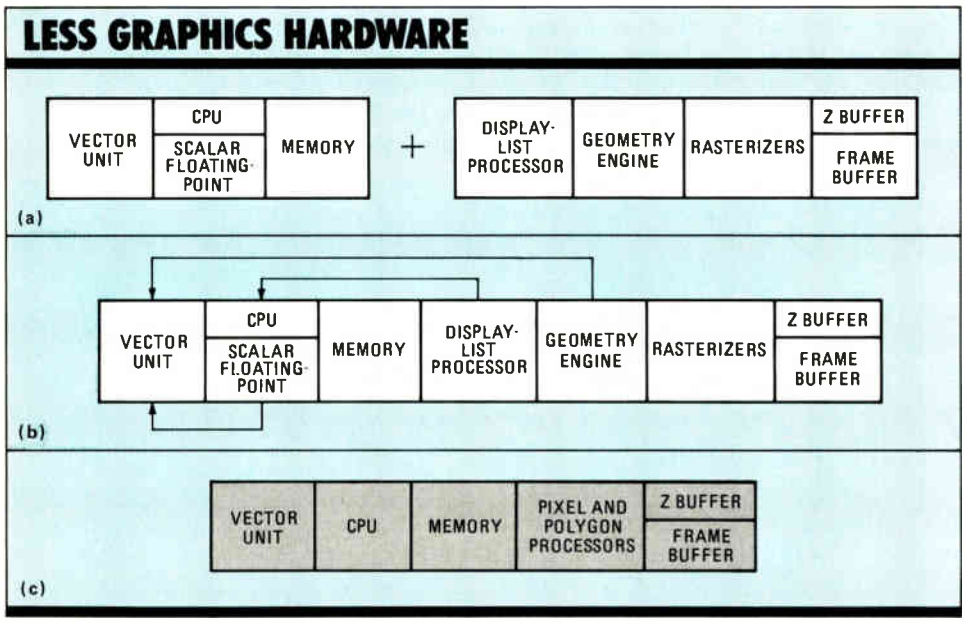
"The problem is to keep the order that these instructions execute in while they are being overlaid," says Miranker. One solution is to serialize the load and store operations, a process which consumes 2n units of time, where n stands for the number of clocks required to perform an operation. The other solution, used in Titan, is to execute the three instructions on an element-by-element basis, which consumes n+1 units of time. "Our solution doubles the rate at which the vector processing unit can compute," Miranker says.

As the value in element 0, vector register 1 is being added to the value in element 2, vector register 2, it is immediately stored in vector register 3. At the same time, the next value is being loaded into element 0, vector register 1. Because other architectures cannot address elements within a vector, they cannot perform overlapping on an element-by-element basis.

Titan's synchronous split-bus architecture allows the system to transfer 128 bits of data every clock cycle, thereby affording a sustained bus transfer rate of 256 Mbytes/s. That's almost 50% better than the fastest minisuper.

One branch of the split bus is devoted to loading the vector unit. The other branch is used for all the bidirectional transfers between memory and the vector unit, integer unit, graphics subsystem, and input and output ports of the system. The vector and integer units each have separate paths to the bus so they can run asynchronously, but the integer unit is tightly coupled to the vector unit.

The integer unit connects to a separate instruction and data caches. For writing, the integer unit has a 4-word-deep write pipeline that buffers write operations from the processor. The processor puts a write operation



2. A conventional supercomputer with a graphics terminal (a) and a graphics-oriented work station (b) needs more hardware than the Titan (c), where the integer and vector processors perform graphics functions.

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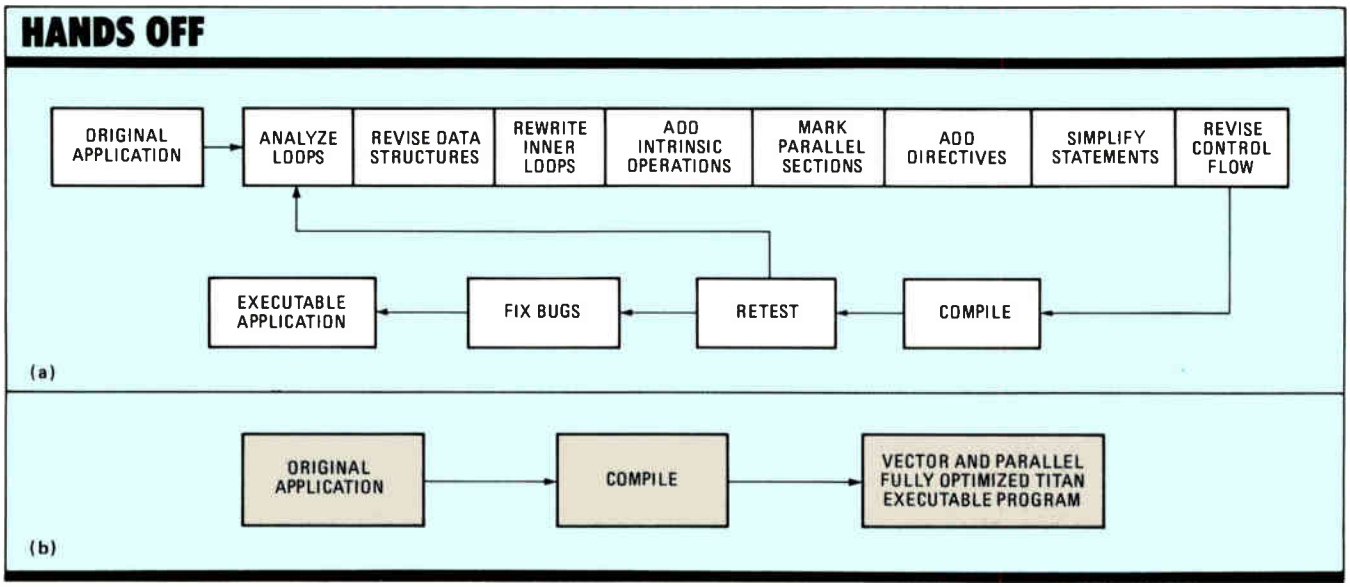

3. Adapting a program with a conventional compiler (a) requires much more hand work than with Titan's optimizing compilers (b).

in the pipeline and continues processing while the buffer writes the data to memory.

A separate bus watcher guarantees that if memory is changed and there is a value in cache which was affected by the change, the cache is invalidated. This removes from the compilers and operating system the chore of monitoring the write-through cache to see that it contains the most up-to-date data.

To display data processed by the four processor boards, Titan comes with a high-performance graphics subsystem that uses much less hardware then either a supercomputer and attached graphics terminal, or a conventional graphics-oriented work station (see fig. 2). In Titan, the vector unit performs the geometry-engine function and the integer processor performs the display list operations.

The vector processor performs graphics functions such as 4-by-4-matrix transformations. The fast RISC integer processor performs graphics operations requiring integer operations such as display-list processing. In addition, the display-list processing itself can be further parallelized to run on all four RISC processors at once. The vector processor also formats and passes commands to the pixel and polygon processors.

After the image has been processed by the vector and integer processors, it is sent to proprietary pixel and polygon processors. "The pixel and polygon processors are supercomputers that have been dedicated to performing the rendering, polygon fill, translation, and other graphics operations," says Bell.

The graphics subsystem contains eight parallel pixel processors, two expandable polygon processors, and 24 image planes that can be organized as a doubled-buffered 8-bit frame buffer. It also has a 16-bit Z-buffer with four overlay planes and three control planes.

An expansion board adds another 32 color planes that provide 48 image planes for double-buffered 24-bit full color. To produce a full-color image requires the 24 bits of data to describe every pixel on the screen. The expansion board also contains four additional pixel processors and another polygon processor.

The Titan gets its power not only from its hardware technology, but also from its software. New Fortran and C compilers can analyze programs written to execute instructions serially and from this analysis, detect opportunities for using vector and parallel operations. A loop that has been fully vectorized and parallelized by the compilers can run as much as 10 times faster. Before the advent of optimizing compilers, the programmer had to perform the vectorization and parallelization operations himself (see fig. 3).

There are three opportunities for the compiler to improve processor performance. It can compile code to execute in parallel on the four processors in the system. It can change integer operations into vector operations. Or it can assign tasks to the integer processor in order to offload the vector processor. It can do this because the asynchronous operation of the two processors means the integer processor can perform bookkeeping operations in parallel with vector operations on the vector processor. "For example, the integer processor can prepare the next vector operation, while the current vector operation is still being completed," says Steve Johnson, Ardent's vice president of software.

"These new compilers can analyze programs better than even traditional compilers used on scalar computers," says Johnson. "We are discovering that even for those loops which are not amenable to vectorization we are able to produce better code because of the information that the compiler is able to discern about the program from this analysis."

For some loops, the compilers split the program loop into vector and nonvector parts and vectorizes the former. Another technique the compilers use is to replace a call instruction to a subroutine with the subroutine itself. This saves the cost of time-consuming call-and-return instructions. While this adds instructions to the basic program, in many cases having the subroutine in the main program allows many more statements to be vectorized. □

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SURPRISE! APOLLO UNVEILS A 'DESKTOP' SUPERCOMPUTER

The series 10000 is a true 64-bit work station, and it's built around a RISC architecture called Prism that the company claims can do something no other RISC system has done so far: execute more than one instruction per machine cycle

by Lawrence Curran

Interest has been building in recent months over the imminent arrival of a new class of supercomputer, called the 'supercomputer on a desk' or the single-user model. Most observers expected the first such product to come from either of two startups, Ardent Computer Corp. or Stellar Computer Inc. But a surprise entry has shown up. Apollo Computer Inc. is launching a new work station this week that racks up an impressive list of industry firsts as it puts supercomputer power at the disposal of a single user.

The new series 10000 from the Chelmsford, Mass., company is built around a reduced-instruction-set architecture that the company calls Prism, for parallel reduced-instruction-set multiprocessor. Among other things, the Prism design makes the 10000 the first RISC system to hit an execution rate of more than one instruction per cycle, according to Terry Condon, marketing manager for high-performance systems, who says the 10000 executes 1.2 to 1.3 instructions per cycle. The RISC systems currently available, from companies such as Hewlett-Packard, MIPS Computer Systems, and Sun Microsystems, strive for one cycle per instruction but so far need two or three cycles.

The 10000 has also racked some other firsts. It's the first work station with a true 64-bit system architecture, including central processing unit, floating-point unit, and system buses. It is the first work station to use scan path technology, which provides a built-in system for testing dense VLSI arrays. Finally, Condon claims his new machine scores a breakthrough in its Linpack benchmark performance: $10,000 per megaflop, compared with about $100,000 per megaflop for conventional supercomputers.

The 10000 is also one of the two first single-user supercomputers; the other is Ardent Computer Corp.'s Titan (see p. 65). Ardent apparently will win the race to market—it shipped preproduction models in February and plans to deliver production models in May. Apollo expects to ship two versions of the 10000 in the third quarter: a server system without a display, which will sell for just under $70,000, and a computational work station offering 1,024-by-800-pixel-by-8-plane graphics, priced just under $80,000. However, the 10000's three-dimensional-graphics subsystem will not be available with the first models. Design work on the subsystem started after the CPU design, so the subsystem will ship a few months later.

The work station alone, though, represents a major commitment by Apollo to its new RISC architecture. Apollo expects that the Prism architecture can accommodate up to three future generations of its hardware over the next five to 10 years, with performance conceivably tripling every two years or so as successive iterations of semiconductor technology are incorporated into it. In the 10000, Prism is implemented in CMOS gate arrays, with custom emitter-coupled logic in its floating-point processors. The system can deliver double-precision Linpack performance of 6 megaflops per CPU, or 9 megaflops in single precision.

Prism is based on what Apollo calls "industrial-strength" RISC. As in other RISC systems, Prism implements the instruction set in hardware, with fixed-length instructions and delayed branching. Where Prism differs is in delivering single-cycle execution. Virtually all instructions are executed in one machine cycle.

One important reason Prism can execute an instruc-

The Apollo series 10000 single-user supercomputer, which implements a RISC architecture called Prism, fits handily upon and under a desk.

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tion per cycle is the substantial local parallelism among processors in each CPU. And the 10000 can support as many as four independent CPUs, each of which has its own floating-point processor, integer unit, dual cache memory, and memory-management unit. Those elements use system-wide 64-bit data paths and registers, which minimize the machine cycles required per instruction. That makes it possible for most double-precision IEEE

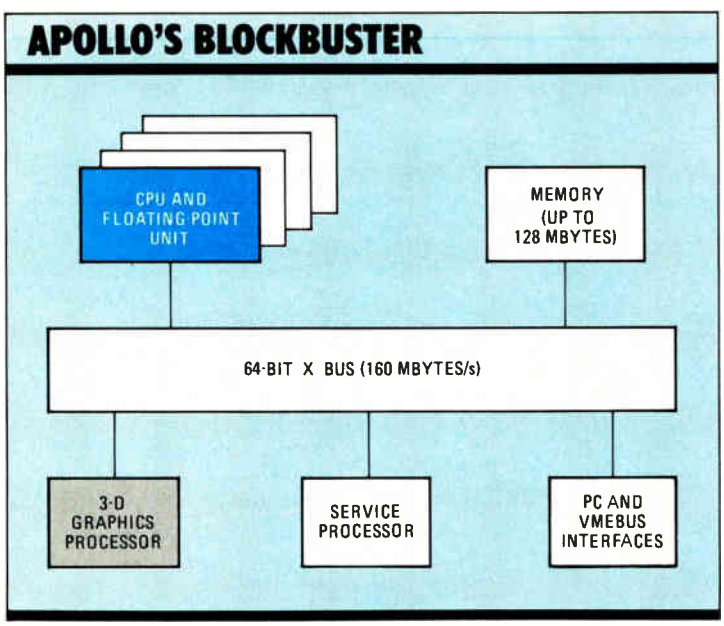
Apollo expects that Prism will serve as the foundation of as many as three generations of its hardware over the next five to 10 years

754 floating-point operations to be processed in a single cycle. A fast—150,000-Mbyte/s—CMOS system bus called the X bus links the CPU, memory, and graphics subsystems (see figure).

The integer processor is a 1.5-μm, 40,000-gate, semicustom RISC-based CMOS array. The floating-point unit's semicustom CMOS register file is combined with the ALU and multiplier, both of which are implemented in custom ECL for high speed.

Each CPU's independent integer processor is coupled with the floating-point unit. These two are peers, which eliminates the software overhead associated with floating-point coprocessors. Because of the peer relationship, floating-point instructions can be dispatched in parallel with integer operations, doubling the throughput that conventional coprocessor techniques achieve. In practice, each CPU can execute as many as three operations per cycle. Floating-point divides and square roots, plus integer divides are the exceptions; these require three or four cycles each.

When the graphics subsystem is delivered, it will also fit into, and benefit from, the parallelism of the overall system. Apollo is not yet ready to provide graphics performance benchmarks, such as polygon-



The CMOS X bus is the 150-Mbyte/s backbone of the series 10000, linking the major subsystems in its parallel multiprocessor architecture.

drawing speeds and Gouraud shading numbers. Condon says only that when the 3-d graphics version of the system is announced in mid-1988, "it will offer state-of-the-art 3-d graphics performance that is equal to or better than anything on the market this year or next."

It is known that the 10000 has a short and simplified hardware geometry that executes only the per-pixel drawing functions used by a variety of graphics techniques. The graphics subsystem will communicate with the CPU over the X bus, and is mapped as a virtual device to give the illusion of exclusive ownership of the graphics engine to each program. All higher-level graphics tasks will be executed directly by the CPU, which will deliver transformations, for example, that equal or exceed those of rigid-geometry pipelines. The CPU processes geometries rapidly and still remains a general-purpose, user-programmable CPU.

These functions are implemented in high-speed CMOS arrays rather than in more commonly used microcode, which eliminates one level of interpretation for the microcode.

The graphics subsystem will have a CMOS RISC-drawing engine tightly coupled to a deep, heavily interleaved frame buffer. A small set of pixel-synthesis operations is implemented directly in 25-ns CMOS, better than twice the cycle speed of the 55-ns CPU.

The 10000's dual-cache memory also contributes to single-cycle execution. The use of separate 128-Kbyte instruction and 64-Kbyte data direct-mapped caches means that instruction-fetch operations can be fully overlapped with memory operand access. Further, the data cache completes loads and stores in a single cycle.

Main-memory architecture extends the 10000's parallel design. It is organized into four modules of 100-ns, static column, CMOS dynamic random-access memory. Each module can contain 8 or 16 Mbytes on an independent daughterboard. Each module is further divided into four interleaved and independently controlled memory banks, assuring a bandwidth that can accommodate the 150-Mbyte/s capacity of the system's X bus. As many as four daughterboards can be mounted on each motherboard, up to a maximum memory size of 128 Mbytes.

Apollo's data-flow compiler was also designed to take advantage of the 10000's parallel architecture. The most important compiler element is the scheduler, which maps the order in which instructions are executed to the available hardware to get maximum productivity from each machine cycle.

The 10000 does not include a vector processor, although it offers good vector performance. A large floating-point register file helps it handle the kind of big arrays that are typically done by vector processors. The register file can be regarded as thirty-two 64-bit registers or sixty-four 32-bit registers, giving it the size and versatility to handle large arrays.

The 10000 will run Apollo's Domain/OS operating system—a distributed Unix environment that integrates Unix System V.3, 4.3 BSD, or Apollo's Aegis operating system with the Apollo Network Computing System architecture. All previous Apollo work stations will be compatible with the new machines. □

For more information, circle 482 on the reader service card.

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A NEW TRANSPUTER DESIGN FROM WEST GERMAN STARTUP

Parsytec's cluster architecture transfers data faster between as many as 64 Inmos processors

In one of the first supercomputer efforts to emerge from Europe, Parsytec GmbH is taking a good idea and expanding on it. The Aachen, West Germany, company is building its Megaframe Supercluster around the 32-bit transputer from Inmos Ltd. By clustering transputers and tying them together with the transputer's communication channels, the company's system reaches data-exchange rates fast enough to give it a supercomputer's level of performance.

The Supercluster uses interprocessor communications to split a computing task into many parallel subtasks. These subtasks exchange data and control information over a large number of dedicated, point-to-point communication channels, thereby avoiding the bottlenecking inherent in a bus architecture. The architecture is modular, so more clusters can be added, increasing the system's speed.

The system resembles the Meiko Ltd. Computer Surface [*Electronics*, Nov. 27, 1986, p. 56], another highly parallel, modular system based on the transputer. And like the system from Meiko, a Bristol, UK, company, the Supercluster is expected to compete against minisuper and low-end supercomputers, although the modular architecture means it conceivably could be expanded to a size and speed that would make it the equal of full-fledged supercomputers for a given application.

Parsytec will introduce two Megaframe Superclusters at the Cebit Computer Fair in Hanover, March 16 to 23—a 64-processor model 64 and a 256-processor model 256. The first model 64 will be delivered to the German Society for Mathematics and Data Processing in St. Augustin, near Bonn, at the end of March. The model 256 will follow soon.

The Supercluster is based on the Inmos T800 transputer, which has four communications channels. The transputers are grouped in clusters of 16 (see figure) and linked through a network-configuration unit. Each cluster has a pair of 16-channel communications lines. The clusters, in turn, are grouped in units of four, linked through two network-configuration units, to make the basic 64-processor Supercluster.

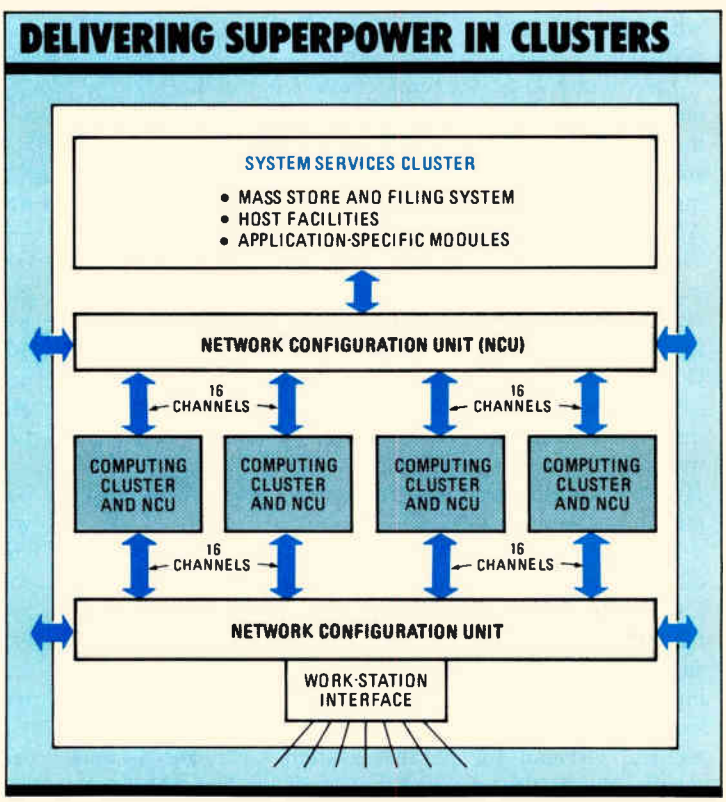
Each unit has work-station interfaces and a system services cluster, which houses the disk-drive filing system, host facilities, and some application-specific modules. Larger superclusters can be formed by connecting two or more basic units through the communications channels emanating from the basic cluster's two network-configuration units.

The basic concept is borrowed from Parsytec's original product, a family of board-level products called the Megaframe-Target series. That product also used transputers in a communication-oriented parallelism, a concept the company is exploiting with considerable success (see p. 72).

Expanding that original idea into a full-fledged system allows the Supercluster to reach "high up in the range of supercomputers," says Falk-Dietrich Kübler, Parsytec's managing director. The members of the new family can be called supercomputers because they deliver very high system throughput for applications written to take advantage of their parallel design, he says. The basic Supercluster's 64 processors together handle 640 million instructions/s and 96 million floating-point operations/s in scalar computations. The model 256's four Supercluster units hit 2,560 mips and 386 megaflops. A faster transputer model, due around mid-year, will considerably boost performance: the 64-processor cluster will then offer 960 mips and 144 Mflops in scalar operations.

Exploiting the transputer's inherent parallelism to get supercomputer performance, rather than using helium-cooled devices or other expensive schemes, also cuts the price of the system, Kübler says. A Supercluster model 64, for example, will sell for $230,000 to $320,000, depending on input/output capacity. That's about a tenth the price of a supercomputer, Kübler says.

A key reason for the price/performance advantage



The Megaframe Supercluster groups 16 transputer-based processors in each of four clusters that are linked through a network-configuration unit.

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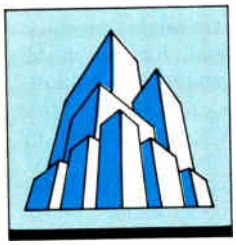
A FIBER-OPTIC LINK THAT RUNS WITH SUPERCOMPUTERS

Aimed at an upcoming ANSI standard, Toplink from Integrated Photonics moves data at 2.43 Gbits/s



The first fiber-optic system that answers an urgent call from supercomputer users for superfast data-transmission links can move data at rates between 405 Mbits/s and 2.43 gigabits/s. The Toplink system from Integrated Photonics Inc., Carlsbad, Calif., is also compatible with emerging standards for high-speed links in development at Los Alamos National Laboratories.

The Toplink system may be the first wave of fiber-optic alternatives for supercomputer environments. The most widely used scheme today for high-speed linking of supercomputers, mainframes, and other machines is the Hyperchannel, a 50-Mbits/s coaxial-cable network from Network Systems Corp., Minneapolis. Network Systems is also developing its own fiber-optic network—to be called Datapipe—which will carry voice, video, and data simultaneously at rates up to 275 Mbits/s.

Toplink is already in the hands of 10 customers, including major computer companies and the Los Alamos labs in New Mexico, where eight Cray supercomputers are installed. Researchers at Los Alamos are working with the American National Standards Institute, which has set up a committee to define the lab's High-Speed Channel for linking its supercomputers.

Integrated Photonics was in close touch with the ANSI group and Los Alamos as they defined their needs, and Toplink is the first system measuring up to the HSC specifications. The HSC program is also strongly backed by major computer firms and industry researchers. The original impetus at the Los Alamos labs came from its Ultraspeed Graphics Project, which required data rates in excess of 60 Mbits/s. The project goal was a standard channel boosting top transmission rates up to 800 Mbits/s.

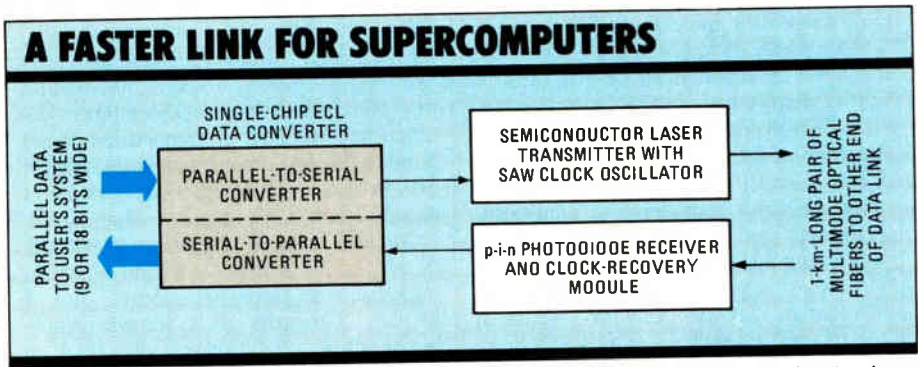
To build Toplink, Integrated Photonics designed electro-optic and ECL data-conversion chips as well as a low-cost multimode laser transmitter (see figure). The Integrated Photonics family may be bought as components or modules, or as a fully packaged three-link-wide unit called Topnode. A single link sells for about $4,500, and Topnode for $9,950. For a bidirectional six-link-wide Toplink, which would operate at the maximum 2.43 Gbits/s, the price is about $36,000. The company plans to offer installation on a board costing about $2,000 in about a year, when it expects demand to start growing significantly as standards are set.

Toplink consists of one to six two-fiber data links, each of which runs at 405 Mbits/s. Six links working together have already been tested at 2.43 Gbits/s. The links use standard optical fiber, either single-fiber or multistrand cables.

The Toplink system is an offshoot of research done at Tacan Co., Integrated Photonics's parent firm in San Diego. At the system's heart is the Parsec-450E, a single-chip parallel-to-serial and serial-to-parallel converter, fabricated in ECL for speed. On the transmitter side of the chip, parallel data is received from a user, converted to serial form for encoding, and passed to the TXC450-M multimode laser transmitter and clock oscillator. The process is reversed on the receiver side.

The data converter runs at rates not possible with discrete parts and the bit-slice architecture allows the flexibility of parallel operation, says Mathieu van den Bergh, Integrated Photonics' director of marketing and sales. Independent logic for the transmitter and receiver allow either dual-simplex or full-duplex operation. The standard interface width is 9 bits, with a double-width option available; when six converters are connected, a 108-bit-wide interface is possible.

The transmitter uses semiconductor laser diodes and has a two-lens scheme for injecting light signals into the fiber-optic cable that is central to its performance and different than other chips for this purpose, says van den Bergh. The oscillator part of the module employs surface-acoustic-wave technology to provide a master-clock signal to the converter chip for system timing. Completing a single-link hookup is the RX450 receiver and clock-recovery module that uses a p-i-n photodiode. More sites will seek data links such as Toplink within a year when generic high-speed networking requirements of 100 Mbits/s are set for minicomputers, van den Bergh predicts. Although the immediate need for networking supercomputers exists primarily at elite research institutions or large computer companies, it marks only a step toward general-purpose use, says Los Alamos' Donald Tolmie, technical coordinator at the labs and vice chairman of the ANSI X3T9.3 committee responsible for HSC definition. *–Larry Waller*



The key to Toplink is the Parsec 450E, a single-chip ECL data converter which sends data to a laser transmitter, allowing data to be moved at a rate of 2.43 gigabits/s.

For more information, circle 484 on the reader service card.

World Radio History

SUPERCOMPUTER SOFTWARE: THE FLOODGATES ARE OPENING

Many of the new budget supercomputers will find application programs ready to go and a lot more software on the way to open up new markets; but new ways must be found to wring better performance from parallel-processing systems

by Jeremy Young

The supercomputer software community is a hive of activity. New hardware vendors are scrambling to produce the longest list of available applications for their machines; researchers at universities and in private industry are sweating away at the programming problems presented by parallel computers; and a move to Unix is underway (see p. 76). And meanwhile, users and potential users everywhere are looking over the new machines and realizing that new kinds of problems can be tackled with them due both to the plummeting cost of performance and to new kinds of capabilities—most notably small, single-user systems that combine number-crunching power with interactive graphics-oriented user interfaces.

Observers who wonder what all the new supercomputers will be used for can rest assured: there are meaningful, profitable uses for these machines. As the product-rollout boom in mid-range and low-end systems proceeds, existing supercomputer users can instantly apply the newly available computation capacity—many of them need just as much power as their budgets will allow. New applications, as they capitalize on falling prices, will in turn drive the market.

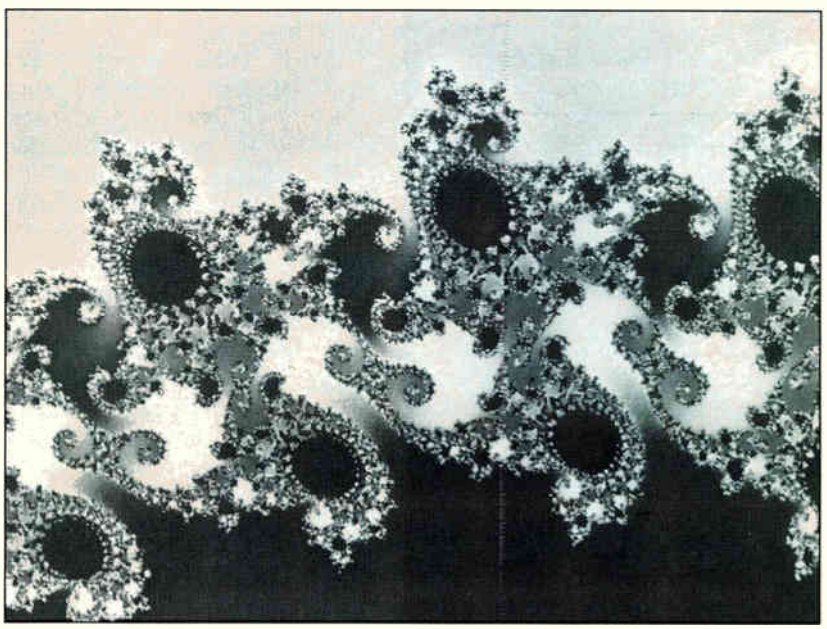
Many of the new machines tie multiple processors together to satisfy growing number-crunching appetites, and software experts are just beginning to find practical ways to make use of these systems. These approaches range from the assignment of each processor to a different program on a multiuser system to what amount to whole new ways of thinking for programmers. Not surprisingly, the easy routes are already being taken; but many of the parallel machines have not yet truly come into their own.

In the short term, the parallel systems with the best chance of making it in the now-crowded market will apply parallel hardware in ways that are invisible to the programmer. These are the systems that can be put to use for existing applications quickly and easily.

Getting applications running on a system is a vital part of any vendor's strategy for selling a new supercomputer, large or small. The customer wants a solution, not a software-porting problem, and if the software he needs doesn't run on a system, he's unlikely to buy it. New supercomputer vendors are now engaged in a dogfight to produce the longest list of available software in the shortest span of time.

Some traditional applications for supercomputers are: structural analysis in mechanical engineering, signal processing, fluid dynamics, simulation, and research in mathematics and physics. Modeling and simulation already represent a very broad set of practical applications; for example, simulating the behavior of electronic circuits is a very power-hungry task. The more computing power that can be thrown at fault simulation, the more complete is the search for possible faults. Chip and system designers are far from satisfied with the amount of simulation they can afford today and will surely welcome the new machines.

One research field that owes a lot to work done on supercomputers is the study of dynamical systems, those exhibiting what appear to be chaotic mathemati-



1. Scientific research relies heavily on supercomputers: for example, pictures of the Mandelbrot set aided the study of chaotic behavior in physical systems.

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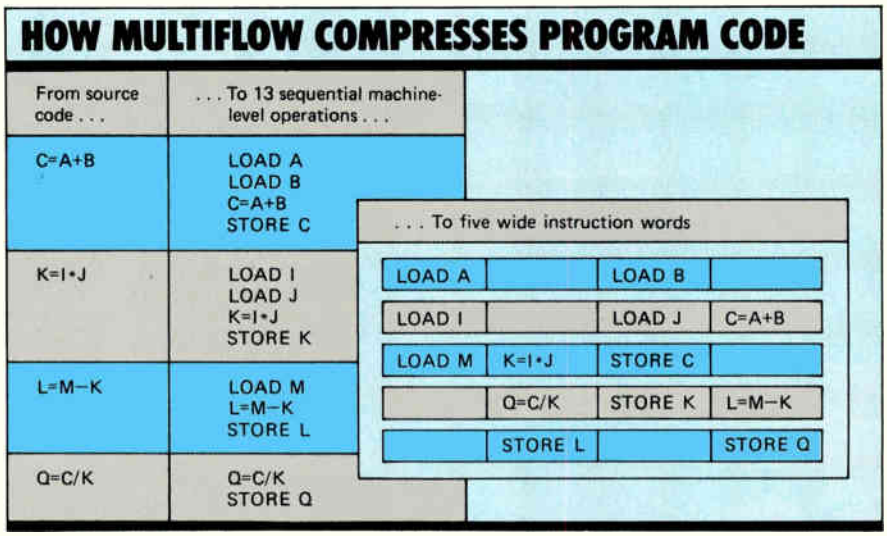
that are cited by supercomputer vendors.

Certain kinds of applications, like fluid-dynamics modeling, are "embarrassingly parallel," as one expert puts it. For these jobs, there is immediate advantage to be gained in using the new massively parallel supercomputers, even if the programs must be rewritten from the ground up. But for other applications, the best way to make use of parallel supercomputers is not always obvious. This question arises most urgently for existing programs, the old but trusted "dusty decks" of computer punch cards.

Much work is being done on compilers that automatically find ways to separate program "threads" that can run in parallel. Convex Computer Corp., Richardson, Texas, for example, will offer later this year a Fortran compiler that looks at a program for opportunities to use either the vector facilities of individual processors or up to four processors at the same time. As programs run, the system will decide on the fly which processing mode—scalar, vector, or parallel—is the best for each block of code.



2. A system with multiple processing elements built into one wide-instruction-word CPU can do highly parallel processing without the need for parallel programming.

But this doesn't always work. "Some kinds of code are highly suited to the implicit mode" in which the compiler makes the decisions about parallel processing, says Robert Paluck, president and chief executive officer of Convex. "Other programs need explict statements" added to them by programmers to take full advantage of parallel processors, he says.

Parallel programming is "at a very embryonic stage," says analyst Smaby. "Though there are a lot of parallel processors out there, most are not running parallel code." Of Cray Research Inc.'s installed base of parallel systems, for example, "only a handful are running parallel code with any regularity," he says.

Most such systems are executing one program each per processor, not putting multiple processors to work on one program. Cray expects to have its autopartitioning capability for parallel processing in a Fortran compiler for the upcoming Y-MP system available about mid-year. The approach "will carry us through 8- or 16-processor machines," says Robert H. Ewald, Cray's vice president for software development. But for systems such as the planned 64-processor Cray-4, a fresh approach will be needed, he says.

The automatic exploitation of parallelism may not extend beyond systems with relatively few processors, for the near term. Massively parallel systems need parallel programming. New computer languages developed for parallel programming, or extensions to existing languages like Fortran, Ada, and C, must be used. New instructions to implement fork and join operations, for example, let the programmer direct the flow of his code on multiple processors.

Thinking Machines Corp. of Cambridge, Mass., is one company that has developed tools for this kind of programming, tools essential to the company's 65,536-processor Connection Machine. "In a lot of ways, [parallel programming] is a more natural way to program than sequentially, but it still requires a change in thought patterns," says W. Daniel Hillis, cofounder of Thinking Machines. "Another generation of people who went to universities using parallel processors will be the pioneers." This will not happen overnight, and Hillis admits that it's a "big disadvantage" right now to have to recode software in a parallel language.

Currently, "the biggest obstacle that [parallel computer] vendors face is in learning how to take advantage of the parallel hardware and still maintain the link" with existing application programs, says Smaby. Companies like Cray and Convex are tackling this problem through compiler technology, but at least one company, Multiflow Computer Inc., Branford, Conn., started with a new compiler technology and designed a parallel system to take advantage of it.

Multiflow's systems can perform up to 7 or 14 operations at a time, depending on the model; a 28-operation system is on the way. But from the user's point of view, they look exactly like standard single-processor computers. The parallelism is achieved through very long instruction words that control multiple processing elements within a single central processing unit. The compiler crams as many parallel operations into each instruction as possible (see fig. 2).

The Multiflow systems also use a technique called trace scheduling, which takes advantage of the parallelisms inherent in ordinary programs. The compiler breaks a program into traces that contain more opportunities for parallel processing because there are no program branches within them, and then carefully schedules the compilation of the traces. Most parallel machines achieve the bulk of their performance gains for software that manipulates big vectors or arrays of data; the Multiflow approach also works well for ordinary—and far more common—scalar routines.

Not all new mid-range and low-end supercomputers have such a strong solution to the dusty-deck problem. But as a group they offer exciting new levels of performance at good prices, and promise to stimulate the development of an entire new generation of application software for a greatly expanded body of users. □

World Radio History

MILITARY/AEROSPACE NEWSLETTER

SIMULATORS GAIN GREATER ROLE IN FLIGHT TRAINING

The Air Force is cutting in half the number of aircraft used for training and relying more heavily on simulators to train fighter pilots and gunners. "It used to be that 25% of all our aircraft were for training, but now we're going to 12.5%," says Randy Olson, the chief Air Force engineer for the F-15E Weapon System Trainer, a key part of the Air Force strategy. Simulators cost less and can support more students than real aircraft. The first version of the F-15E trainer, which is being built by Loral Defense Systems of Akron, Ohio, will go into test in April and is scheduled for delivery to Luke Air Force Base in Arizona this summer. The $30 million system, which includes five mainframe computers and 25 video displays, will get a real workout: the Air Force expects eight flight crews to work two-hour shifts on the simulator every day. □

EVEN IF THE LHX HELICOPTER DIES, ITS COCKPIT WILL LIVE ON

The Army is deferring its most advanced helicopter project, the LHX (for Light Helicopter Experimental), because of budget problems (see story, p. 32), but the advanced cockpit that was an extension of the LHX program will likely be its legacy. "Even if the LHX dies, there will be follow-ons for other helicopters and other aircraft," says Dean Kocian, an engineer in the Visual Display Systems Branch of Wright Patterson Air Force Base, Ohio. That group has been working on a cockpit system that would superimpose critical flight information on the visor of the pilot's helmet, along with an animated, panoramic display of his surroundings. Kocian says his group has made great strides in developing prototype displays for the system, including tiny 0.5- and 0.25-in. high-intensity cathode-ray tubes and the optics needed to project images on the visor. Still missing, however, is a high-speed graphics processor that can handle the tremendous throughput the cockpit requires. □

REDESIGN DELAYS AIRBORNE SELF-PROTECTION JAMMER

The biggest production run of electronic warfare systems in U. S. history won't get off the ground as quickly as planned. The Airborne Self-Protection Jammer, an internally mounted radar-jamming system for the Air Force's F-16 and the Navy's F-14 and F-18 fighters, is being redesigned to simplify manufacturing and maintenance, delaying it by up to two years. Westinghouse Electric Corp. and ITT Corp., which jointly developed the system and will eventually compete for production orders, are now replacing hybrid circuits with 1.5-μm and 2.0-μm gate arrays in order to make the system more portable from one aircraft to another. Each plane allots 2.5 cubic ft. for the system, says Robert Jolin, marketing manager for the Electronic Warfare Division at Westinghouse in Baltimore. But the form factor for each plane is different. Switching to gate arrays, he says, will save space, boost reliability, and ultimately cut costs. The Navy and Air Force together will buy about 3,000 of the systems, at a cost of about $1.3 million to $1.5 million each.□

THE PENTAGON PLANS TIGHTER CONTROL OVER CRYPTOGRAPHIC KEYS

GTE Government Systems of Waltham, Mass., will develop a cryptographic-key management system for the Defense Department as part of a project aimed at protecting both government and commercial data transmissions. GTE's Electronic Defense Communications Directorate will deliver the $39.6 million secure-key management system in about three years. It will be used to control the issue of cryptographic keys for military computer equipment being developed by various independent vendors as part of the Secure Data Network System, which will provide low-cost security for classified or sensitive data transmissions. □

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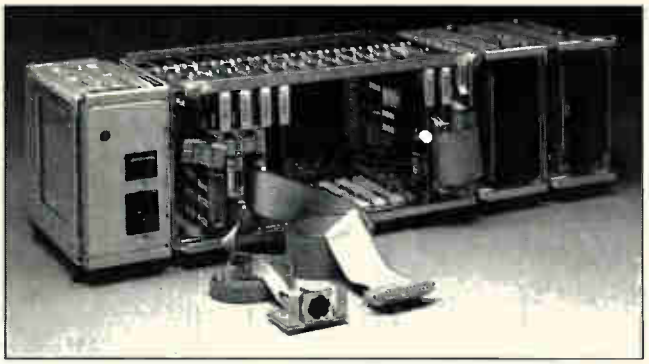
NEW PRODUCTS

PRO-LOG'S FACTORY COMPUTER DELIVERS PC-AT POWER ON A 16-BIT STD BUS

Parallel architecture and MS-DOS 3.3 double existing 8-bit STD bus performance

Pro-Log Corp.'s System 2 Model 30 Industrial Computer uses a 16-bit STD bus and a parallel-processing architecture to deliver up to twice the performance of conventional 8-bit STD bus computers, while maintaining compatibility with IBM Corp.'s Personal Computer family.

An 8086-compatible CMOS microprocessor and an MS-DOS 3.3 operating system combine to provide performance comparable to an 8-MHz IBM PC/AT, Pro-Log maintains. The company's proprietary Multimaster shared-access bus arbitration scheme provides added throughput. Up to seven additional processors plug into the rugged rack-mounted system to provide concurrent parallel processing based on other operating systems or based on executable code for specific real-time, input/output-intensive tasks.



Up to seven additional processors plug into the rack-mounted system to provide parallel processing based on different operating systems.

Using optional peripheral cards from Pro-Log or about 100 other manufacturers, the System 2 Model 30 can be customized for use in robotics, machine control, data acquistion, test and measurement, and other harsh factory jobs, says the Monterey, Calif., company.

CARD RACK. The company's BX-Series Card Rack provides an STD bus backplane for up to 30 configurations using up to 26 cards. Since at least one processor in the system always runs MS-DOS, data from other real-time processors can be passed through a shared memory scheme for manipulation, report generation, and other operator tasks using available PC-compatible software.

"The real benefit [of the Model 30 architecture] is going to come in dealing with real-time I/O," says Paul Virgo, Pro-Log marketing director. Compared with PC-based factory solutions that rely on multitasking software to handle tasks in a certain sequence, "you can divide those tasks up and give them each their own processor, so that they run uninterrupted, and obviously a lot faster," Virgo says. And thanks to the mechanically robust and vibration-resistant construction of the 4½-by-6-in. STD-bus form factor, the Model 30 can be embedded in factory equipment more easily and more reliably than computers based on the PC bus or alternative bus schemes, Virgo adds. The Model 30 is backed by a five-year warranty, compared with 90-day warranties typical of IBM's industrial PC family, he says.

Depending on the application, the Model 30 will also run up to twice as fast as other STD bus-based industrial computers, which rely on 8-bit data transfers, says product marketing manager Mary Healy. "Other STD vendors have incorporated 16-bit processors, but have maintained the 8-bit bus," she says.

A basic System 2 Model 30 costs $1,495 and consists of two cards: a 7891 16-Bit V30 Multimaster CPU Card and a 7171 System Support Card. "Between them, they have all the peripherals that DOS requires, plus 128 Kbytes of memory and a 10 MHz V30 microprocessor," Virgo says. (The V30, supplied by NEC Corp., is a CMOS 8086 equivalent.) Additional processor cards can be added at a single-unit price of $845, while a CPU equipped with an Intel Corp. 8087 math coprocessing chip is also available, priced at $1,290. MultiBASIC, a multitasking control language developed for Pro-Log's System 2 family by General Digital Corp., Manchester, Conn., is priced at $995 for a single copy.

Program development can be done with the configuration that provides full PC/AT emulation. This version of the system sells for $5,500 in a desktop- or rack-mounting enclosure. It incorporates 640 Kbytes of system memory, an EGA board, serial and printer interfaces, a 720-Kbyte, 3½-in. floppy-disk drive, a 360-Kbyte, 5¼-in. floppy-disk drive, and a 30-Mbyte, 5¼-in. hard-disk drive. The System 2 Model 30 will be available April 1. – *Wesley R. Iversen*

Pro-Log Corp., 2560 Garden Road, Monterey, Calif. 93940.
Phone (408) 372-4593 [Circle 460]

COGNEX'S MACHINE VISION: LOW COST, SHARPER SIGHT

Manufacturers of automated equipment for loading printed-circuit boards or assembling hybrid circuits can cut their machine-vision costs at least in half with Cognex Corp.'s model 1500. The company claims it is the first mid-range machine-vision system—an alternative for users who find low-end systems inadequate but do not need all the power of the $20,000-to-$40,000 vision systems on the high end.

The 1500 costs less than $10,000 in volume quantities. However, it can actually identify objects, unlike low-end systems, which lack discrimination. They detect and locate an object, but do not tell the host processor what it is.

The low cost is possible because the system's software and hardware are tailored for locating and aligning objects. Also, the 1500 is driven by the host computer or microprocessor that controls the automated equipment. Higher-priced systems usually incorporate their own pro-

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cessor and software, which adds to the cost. The host processor can be an automated driller, laser trimmer, screen printer, or component-placement machine.

A complete 1500 includes a rack-mountable chassis, solid-state video camera, monochrome monitor, trackball, cables, and documentation. The chassis houses a vision processor incorporating a Motorola Inc. 12-MHz MC68000 microprocessor, an image digitizer with a resolution of 576-by-448 pixels with 64 gray levels, a vision coprocessor, and memory.

The 1500 locates objects and features by gray-scale pattern matching. At setup, an operator trains the system to identify a pattern by showing it a part and using the trackball to draw a box around the feature of interest. Digital logic evaluates all possible object positions within the viewed image and determines the part location that is in the position representing the best match.

Processing time ranges from 0.05 to 0.5 s. System accuracy is within 1/2000th of the camera's field of view; the sensor's absolute accuracy depends on the resolution of the camera lens. Shipments begin in May. *–Lawrence Curran*

Cognex Corp., 72 River Park St., Needham, Mass. 02194.
Phone (617) 449-6030 Circle 461]

SOFTWARE ENABLES EEPLD DESIGNERS TO USE FAMILIAR TTL

A new TTL macro-design library for electrically erasable programmable logic devices from Exel Microelectronics Inc. boasts more than 100 standard TTL building blocks and a set of algorithms to optimize circuit functionality.

The new EEPLD-programming software for Exel's electrically reprogrammable application-specific integrated circuits, or ERASICs, features four logic-packing algorithms that eliminate unused logic in each TTL macro and reuse it when possible in other functions. The software allows EEPLD users to work with familiar TTL macros, but cuts out excess logic for one-chip designs.

The stingy logic-packing routines are global-term sharing, merging, fixed 0/1 reduction, and dangling logic removal. The sharing algorithm checks design for TTL-defined functions that contain the same terms. In merging, software checks cascaded gates to see if combinations can be reduced to one level of circuit. For example, a NAND gate followed by a NOR "can be represented by one big NOR," says Erich Goetting, EEPLD program manager.

In addition, the fixed 0/1 reduction

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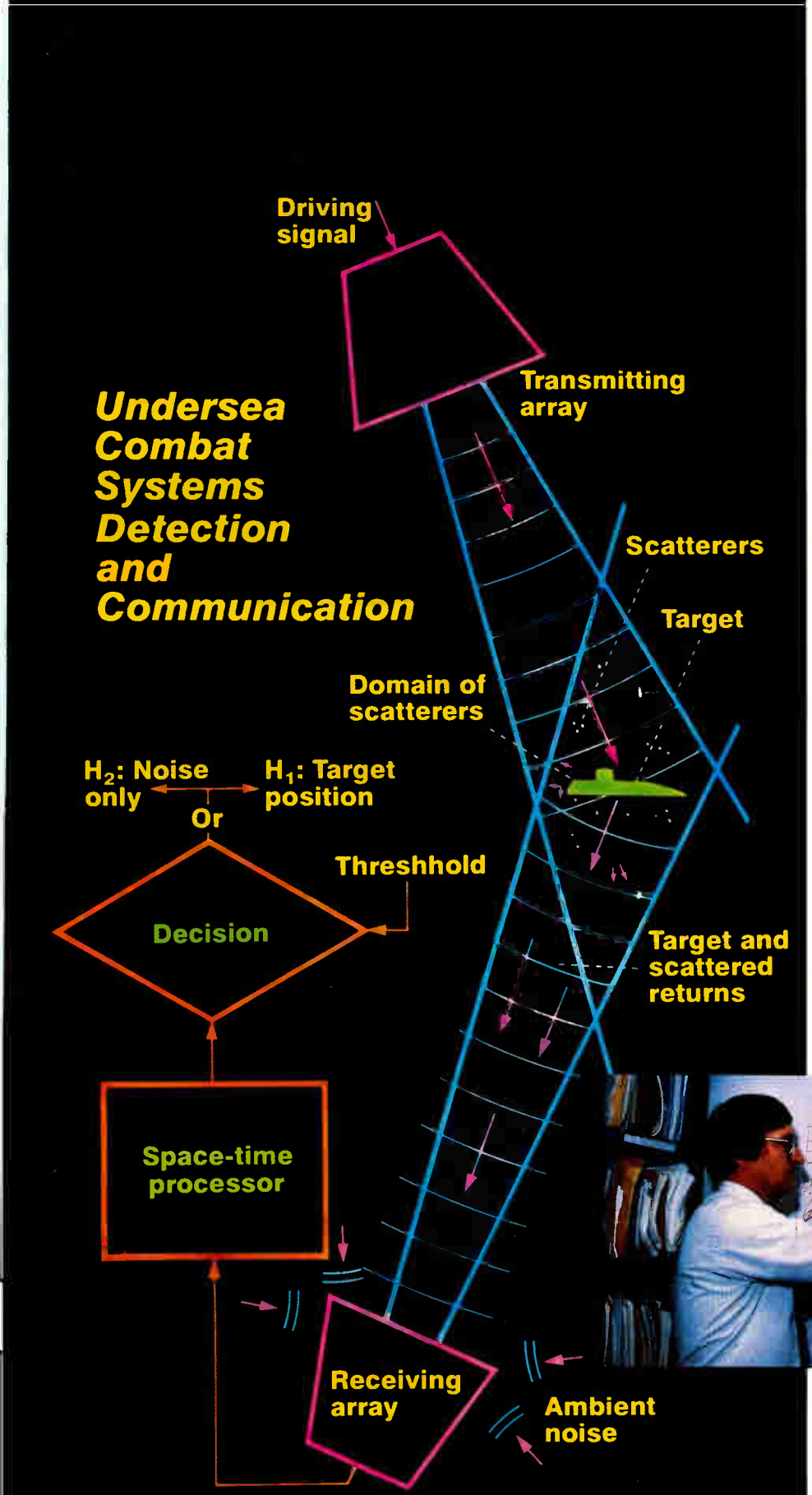

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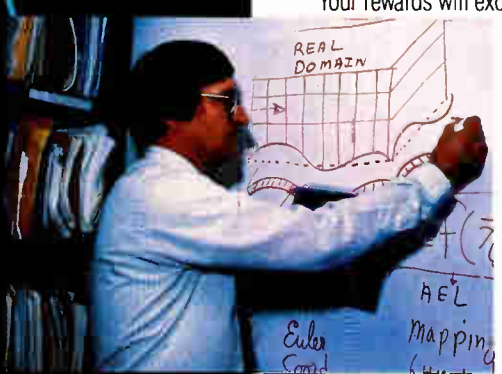

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fered by NCR Corp., Logic Devices says, the L53C80's speed will help to extend the life of today's asynchronous SCSI products. The device achieves up to 4-Mbyte/s transfer rates in asynchronous SCSI systems, which is double the speed of equipment using competing integrated circuits. A few minor changes in surrounding logic are required to get the overall performance boost.

The Sunnyvale, Calif., firm's 1.5-μm double-metal CMOS process produces chips with 48-mA drive required by SCSI systems. The chips support high speeds without generating glitches from internal latchup or ground bounce, which have plagued other designs in the past, says Joel H. Dedrick, director of product development. The L53C80 also corrects eight known bugs present in NCR's year-old CMOS parts. One bug, for example, prevents system designers from using the block-mode direct-memory access feature of SCSI.

"Much of the speed comes from our process and changes to the internal state machine that handles protocol handshakes between peripherals and central processing host," Dedrick says. The lion's share of the design-oriented speed advantages are implemented in

The L53C80 handles 4-Mbyte/s transfers without glitches or ground bounce.

the transactions between the host and the controller, such as speeding up the access between the SCSI chip and processor memory.

The chip contains all of the features to support asynchronous SCSI as defined by ANSI's X3T9.2 committee in the X3.131-1986 specifications. It works in both initiator and target modes, making it suitable for computer hosts or disk drives.

While twice as fast as competing CMOS chips, the L53C80 consumes no more power—just 50 mW with a 5-V supply. The 4-Mbyte/s SCSI chips are available in 48-pin plastic dual in-line packages and cost $9 each in 100-piece quantities. – *J. Robert Lineback*

Logic Devices Inc., 628 E. Evelyn Ave., Sunnyvale, Calif. 94086.
Phone (408) 720-8630 [Circle 361]

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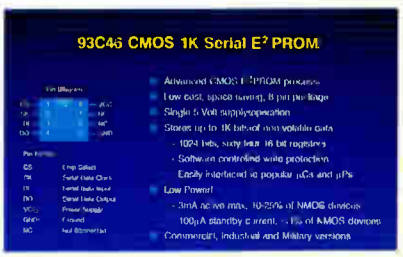

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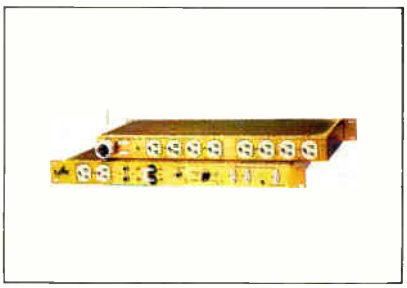

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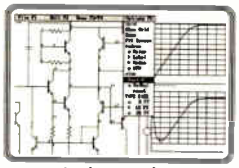

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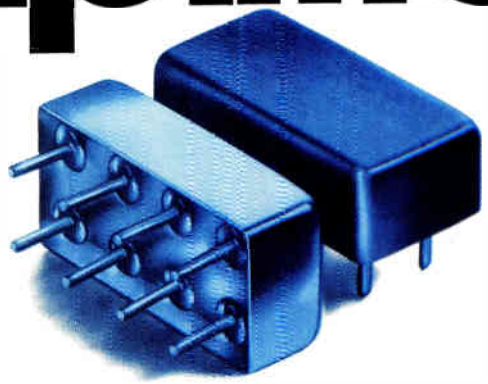

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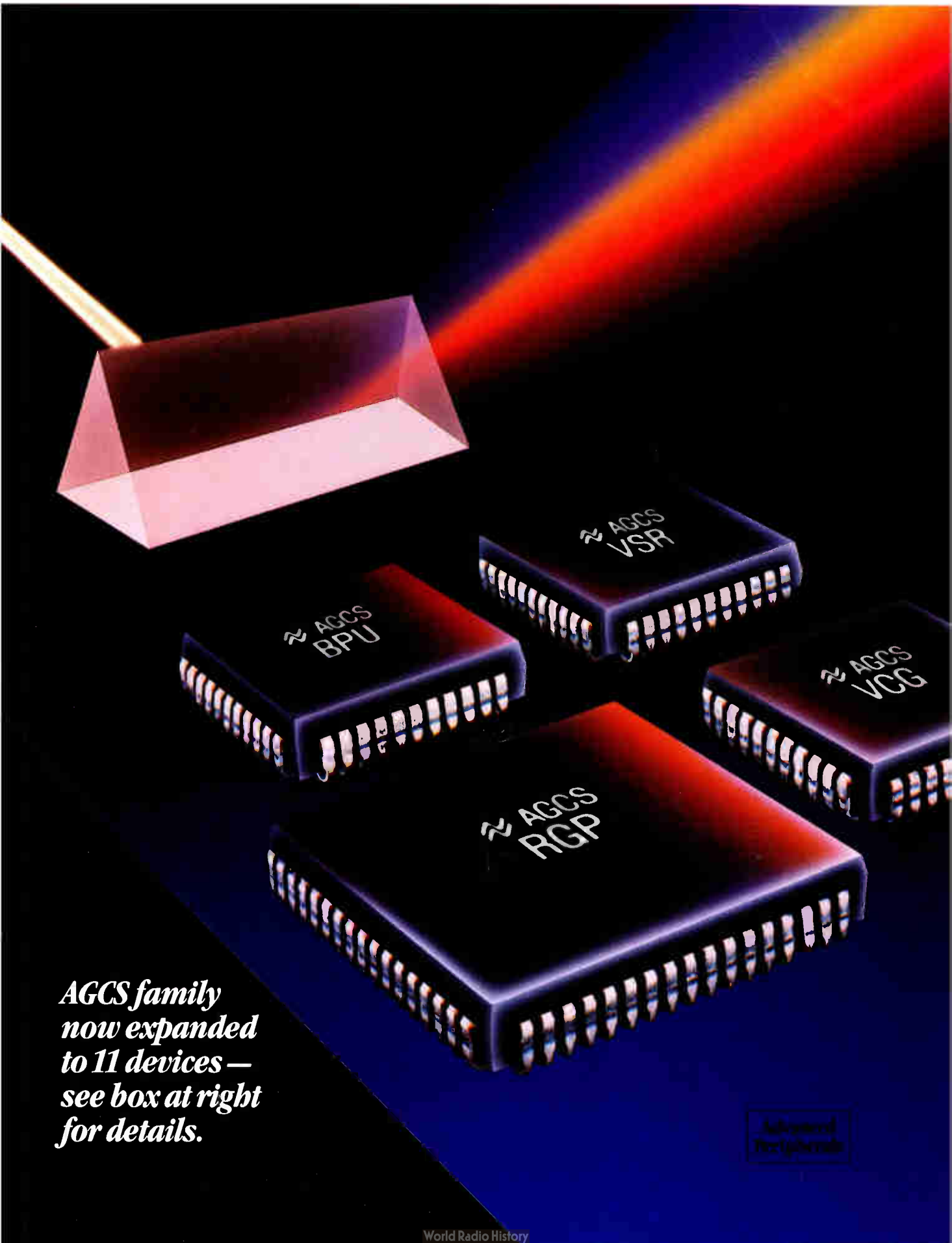

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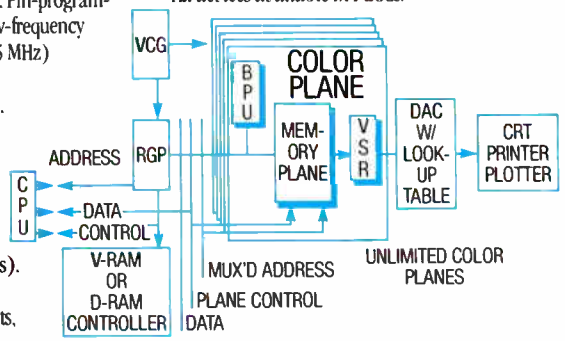

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Anyone who has been in the news business for any period of time knows that the story doesn't end just because it has seen print. There always are continuing new developments to be reported, new angles to be covered.

No one knows that better than *Electronics*. For example, last year we published two special issues on the semiconductor industry—two issues that, by the way, have won two major editorial excellence awards. The first, "The Chip Makers: Where They're Heading," appeared on April 2. Then, four months later, on Aug. 6, we dug into "The ASIC Takeover." But we're not about to stop there. There have, of course, been further developments, and in this issue, *Electronics* mounts a three-pronged investigation that may be considered an extension of those two special reports from last year.

The first, starting on p. 67, is a special nine-part series on the International Solid State Circuits Conference, going on this week in San Francisco. With semiconductors editor Bernie Cole spearheading the operation from his base in San Mateo, and executive editor Sam Weber running the show in New York, the package parallels the ISSCC's technology tracks. Moreover, it once again shows how *Electronics* is able to deploy its team of seasoned editors to blanket a breaking story.

Included are contributions from Cole, Larry Waller in Los Angeles, and Tobias Naegele and Stan Runyon in New York. The articles run the semiconductor gamut, from memories to converters, logic to processors. As a matter of fact, Bernie describes the 1988 edition of the ISSCC as "a show that will be remembered as one that spotlighted a raft of watershed developments." For example, he says, "There are the new 16-Mbit random-access memories—that's more memory space than some hard disks, more memory space than two floppy drives on an IBM PC.

"Equally exciting are the 1-Mbit static RAMs with 15-to-40-ns speeds. They're as large as the dynamic RAMs coming into production and five to six times faster. That means they can be used instead of the slow DRAM and cache static, and the designer winds up with both high speed and more density." In addition, notes Bernie, there are the algorithm-specific processors that do in hardware what now has to be done in software, thereby saving memory space.

Technology doesn't exist in a vacuum, so even as we describe in great detail the excitement generated by all these advances in chip technology, we are not neglecting the business side of the industry. So the second major part of the semiconductor coverage in this issue—and of our pledge to provide complete and continuing examination of both sides of the equation—is Rob Lineback's Inside Technology on p. 81 dissecting the rarely explored question of profitability. Rob points out that a big question looms over the industry today: is the current disappointingly low return on equity a serious harbinger of bad times on the horizon—or is simply a hangover from the bad times that the chip makers went through in the early part of the decade? This is the takeoff point for his article.

Rounding things out is the exclusive Inside Technology article on p. 83 describing Motorola's hot new reduced-instruction-set-computer chip. Earlier this month, Stan Runyon flew from New York to Texas to join Dallas bureau manager Lineback for a first look at the long-awaited chip. Runyon was impressed. He says, "Motorola's chip could do for the world of RISC what its 68000 family did for the world of CISC."

Laurence Altman

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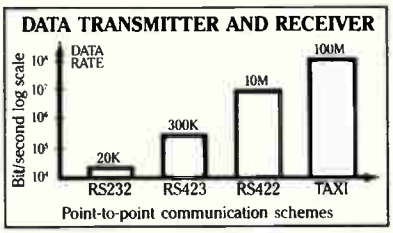

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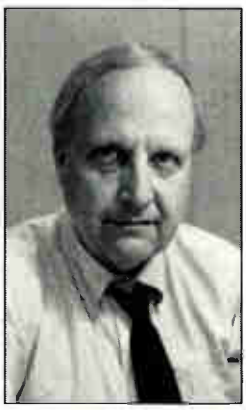
'THREAT OF THE WEEK': COMPUTER VIRUSES

How the "Times" riles us with its doomsday scenario of virulent outbreaks of viruses that can put worldwide computer networks out of commission



I couldn't believe my eyes. In the Sunday *New York Times*, bold headlines proclaimed: "Virus programs that can elude most barriers have begun to infect computers around the world." In what a long, rambling article described as a "science-fiction nightmare come to life," viruses that "subvert, alter, or destroy programs" were reported to have infected personal computers at several places. These viruses were said to be highly contagious, capable of instantaneously cloning copies of themselves and burying them inside other programs. These programs then become contagious and the viruses pass to other computers that come in contact with the infected software. Thus a PC-based electronic bulletin board could rapidly infect thousands of small computers.

As far as I was concerned, the *Times* story itself was a piece of science fiction. At best, it didn't muster nearly enough evidence to back up its scare headlines. Even so, we checked it out. After talking to the experts, we found most believed the *Times* story was "alarmist," but they also agreed such viruses were indeed possible.

A Washington-based expert for one leading consultant who knows about such things says these viruses are "extremely rare." No system he or his people had ever worked on that had a reasonable level of security has ever been attacked by a virus, he maintains. But he did point out that many systems are set up with insufficient security, and that some of the possible forms of attack on these computers are "scary." The main way to avoid such problems, he notes, is to carefully restrict access to a system.

Once such press reports appear, you can look for one of two possible scenarios, says SRI International's Donn Parker, a leading expert on computer crime. "The whole thing can just blow over, just as it did after the publicizing of other computer threats such as rf emanations, hackers, and phone freaks," he says. "Viruses will be just another computer system vulnerability to be wary of." But his worst-case scenario is worrisome: virus attacks will increase dramatically and end up destroying all public domain software, causing what Donn calls the "Tylenol Syndrome." Software will be suspected of contamination and will be avoided, possibly causing the demise of some software companies. While Donn leans strongly toward his first scenario, we are sufficiently motivated to dig into this. Stay tuned. **ROBERT W. HENKEL**

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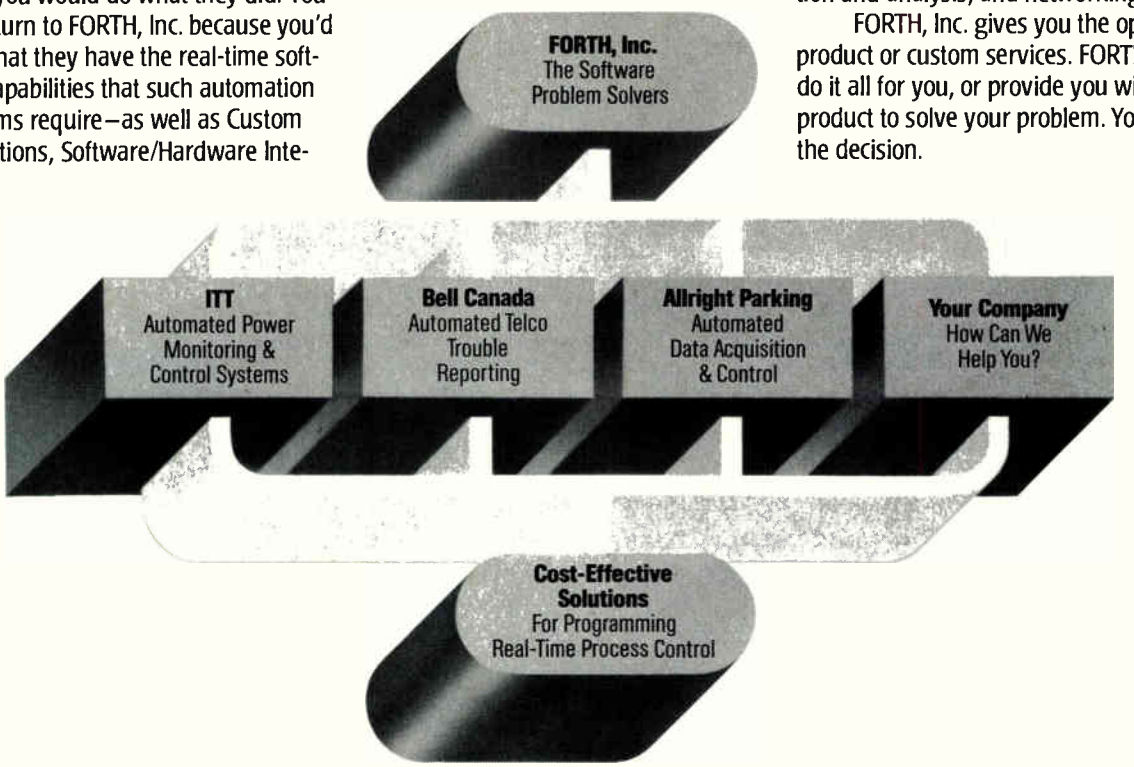

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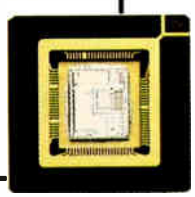

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Circle 15 on reader service card

New high performance PC-based emulators from HP.

Introducing the HP 64700 Series emulators. Low-cost, entry-level, PC-based emulators with features you won't find with any others in the price range—or even higher. The HP 64700s deliver unmatched capability, ease-of-use, measurement power, flexibility, and reliability . . . plus HP support.

While the HP 64700s are tailored to meet the needs of individual engineers and small design teams, they'll perform equally well for large teams working on complex projects.

The rapidly expanding family of HP 64700 emulators provide real-time, transparent emulation at full processor speeds with no wait states. The PC user interface gives a new meaning to the term "friendly" with features like multiple windows, single-letter keystroke command entry, access to symbols for powerful debugging capability, timing diagrams, and on, and on, and on. The experienced user as well as the beginner will appreciate how easy these emulators are to work with.

In addition to the features shown above, there are lots of others that put the HP 64700s in a class by themselves. To name a few: function with IBM-PC, HP Vectra and compatibles, RS-422 high-speed serial

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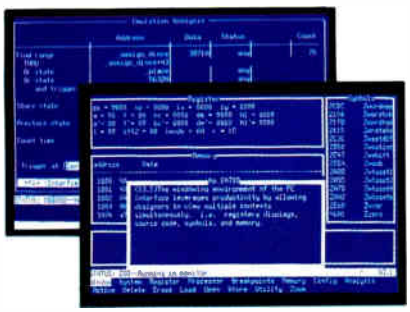
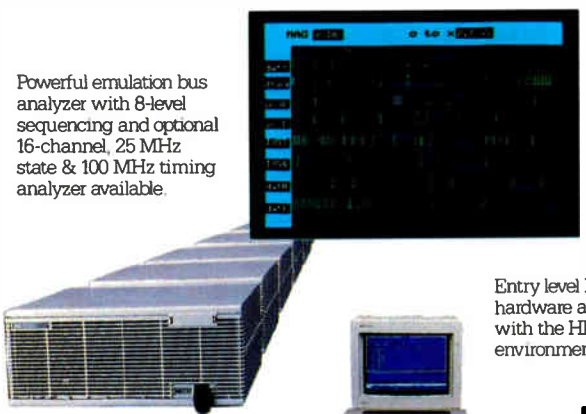


Multiwindow viewing allows up to eight displays on-screen simultaneously.

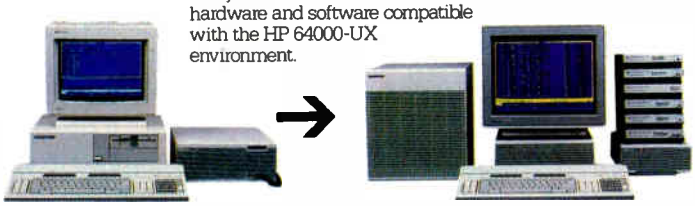
"Sky-hook" handles plus flexible 2- to 3-foot cables and low-profile probes allow easy access into target systems.

Powerful emulation bus analyzer with 8-level sequencing and optional 16-channel, 25 MHz state & 100 MHz timing analyzer available.



Up to 32 emulators can be interconnected, synchronously started, cross armed, cross triggered, and halted.

Entry level HP 64700 emulators are hardware and software compatible with the HP 64000-UX environment.



interface for superior download and upload speed, code coverage analysis for efficient software testing and design, host-independent portability, and compatibility with popular absolute file formats such as Tektronix and Intel hexadecimal and Motorola S record.

Once you get your hands on an HP 64700 emulator, you'll agree that this is the new standard in the field. Especially at a starting price of $8,900.

Free demo disc.

For a free demo disc that gives you the "hands-on" feel for HP 64700 Series capabilities, call HP at 1-800-752-0900 ext. 501A, or mail the attached business reply card.

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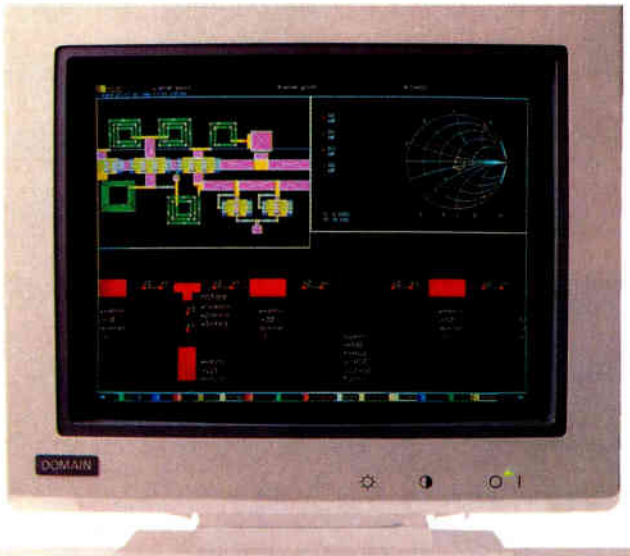

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ELECTRONICS NEWSLETTER

INTEL GETS ON THE SCOREBOARD WITH 10-MIPS CONTROLLER...

Look for plenty of action from Intel Corp. in the embedded processor/controller market in the months ahead. The Santa Clara, Calif., company tipped its hand in a late paper on "scoreboarding" at this week's International Solid State Circuits Conference in San Francisco. In the proprietary technique, registers keep track of outstanding read accesses as the processor continues to execute other instructions. This overlapping scheme, Intel designers say, significantly improves performance and reduces the effects of slower external memory. The scheme will be one of the reduced-instruction-set features incorporated in a new 32-bit controller family, which will push performance to between 2 and 10 million instructions/s. Intel also has in mind a slimmed-down version of its 80386, a follow-on to its 80186 embedded processor [*Electronics,* Oct. 29, 1987, p. 22]. □

...AND FLASHES NEW EEPROM AT ISSCC

In still another late ISSCC paper, Intel Corp. signalled its entry in the market for flash electrically erasable programmable read-only memories, which until now has been the sole preserve of Seeq Technology Inc., San Jose, Calif. Intel will enter the market with a 256-Kbit double-polysilicon CMOS part that is based on a single-transistor cell. Fabricated with a 1.5-μm CMOS process, the 150-mW Intel device features a 110-ns access time, a 200-ms erase time, and a 100-μs-per-byte programming time. Seeq and Intel won't have the market all to themselves for long, however. A number of other companies have announced that they intend to enter the fray—among them, Exel Microelectronics, Hitachi Ltd., National Semiconductor Corp., and Toshiba Corp. □

AT&T WILL START BRIEFING CUSTOMERS ON VERSION 4.0 OF UNIX V THIS SUMMER

A new version of AT&T Co.'s Unix System V is in the offing for late 1989 and yet another version is taking shape. At last week's Uniforum show in Dallas, AT&T announced it would start briefing computer companies and software developers about Unix System V Version 4.0 this summer. The company also used the show to give licensees a peek at what's in store: Sun Microsystems Inc.'s Remote Procedure Call and Network File System software will be added, along with some features of Microsoft Corp.'s Xenix System V and others that are derived from Berkeley Unix. Meanwhile, Bill Joy, Sun's vice president of research and development, is setting up a group to rewrite the Unix kernel in C++, an object-oriented extension to the C programming language. This kernel will be used in Version 5 of Unix System V, and Joy says it should make the operating system easier for licensees to enhance. □

HONEYWELL-NEC CONTEMPLATES A SUPERCOMPUTER WITH TWICE THE CRAY Y-MP'S SPEED

Cray Research Inc. barely had time to bask in the glow of the Y-MP introduction (see story, p. 31) when rumors surfaced that Honeywell-NEC Supercomputers Inc. (HNSX) is working on a four-processor supercomputer that will double the Y-MP's 6-ns clock speed. At the moment, the HNSX machine is just a cloud on the horizon—a senior HNSX official says the company doesn't have a multiprocessor machine at the moment. "We've been visited in Tokyo by people from some significant laboratories who have been exposed to ideas and concepts, not a machine. No announcement is imminent, but we're in the market to stay if NEC's history of getting into any market is a precedent." A source at NEC admits that the Tokyo company is doing research on a multiprocessor supercomputer but still extolls the virtues of the fastest possible single processor with a large number of parallel pipelines. □

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PRODUCTS NEWSLETTER

HITACHI LIKELY TO BE FIRST TO MARKET WITH 1-MBIT STATIC RAM

Looks like Hitachi Ltd. will be the first to market a 1-Mbit static random-access memory. Although Hitachi's chip seems likely to be outperformed by a slew of 1-Mbit introductions later this year (see story p. 69), its 70-ns access time is fast enough to replace dynamic RAMs in high-end computer systems. Configured as 128 K by 8 bits, the HM628128 will be available in sample form in April with 70-, 85-, 100-, and 120-ns access times. The part is built using 0.8-μm design rules—compared with 1.3 μm rules for the Tokyo-based company's 256-Kbit SRAMs—and a triple-layer-polysilicon process. The 7-by-14.4-mm chip operates at 70 mA, has a standby current of 2 mA, and is TTL-compatible. Devices come in 32-pin dual in-line and small-outline packages. Prices in Japan range from 52,000 yen for the 70-ns DIP to 70,000 yen for the fastest SO units. Export pricing has not been set. □

ANALOG DEVICES TEAMS WITH BROOKTREE TO ENTER GRAPHICS-DISPLAY CHIP MARKET

Analog Devices Inc. will team up with Brooktree Corp. to enter the exploding graphics display market; the duo hopes to establish a video standard. The two companies will independently develop, manufacture, and market RGB (red, green, blue) video digital-to-analog converters for generating analog signals for color displays, says James Bixby, president and chief executive officer of Brooktree in San Diego. Under phase one of the agreement, Analog Devices, Norwood, Mass., will second-source Brooktree's Bt471 and Bt478 RAMDACs, which are, respectively, a triple 6-bit and a triple 8-bit DAC with onboard RAM, aimed at the PS/2 personal computer market. Later, Analog Devices will adapt Brooktree architecture and pinouts to develop its own proprietary products. □

ELXSI'S "SUPERFRAME" BLAZES IN REAL-TIME PROCESSING

Control lines hardwired directly into the central processing unit of Elxsi Corp.'s upcoming 6460 processor will enable the new vector-scalar system to stop on a dime and service external interrupts in less than 10 μs. That beats by 10 times the speed of competing machines, says Peter Appleton Jones, Elxsi's president. Jones, in fact, is touting the 6460 as a new class of hardware—the "Superframe"—that merges the best of supercomputers and mainframe power. The San Jose, Calif., company plans to patent the architecture, which has eight interrupt lines wired into the CPU as opposed to more conventional message systems using firmware and software. Up to ten 6460 vector-scalar units can be loaded into an Elxsi chassis. A fully loaded system will run at 250 million instructions/s or 100 million floating-point operations/s and cost just under $4 million. □

NEC'S IMAGE-COMPRESSION CHIP IS TWICE AS FAST AS THE COMPETITION

NEC Corp.'s image compression/expansion chip for black-and-white applications such as facsimile machines and image work stations doubles the best performance of the competition—and delivers the kind of power needed for storing and retrieving images from optical or hard disks. The μPD72185 gets its speed by using pipeline processing in a four-stage dedicated circuit and a high-speed on-chip CPU. The chip compresses or expands a standard, letter-size CCITT test chart in less than 0.75 s. Facsimile machines using it can talk to almost any other fax because the μPD72185 handles the three most popular compression/expansion algorithms. Image size can also be doubled or halved. The 180,000-transistor device is fabricated in 1.5 μm CMOS technology on a 9.5-by-9.9-mm. chip. Sample shipments will begin in April at a price of 20,000 yen. Production will begin in June. □

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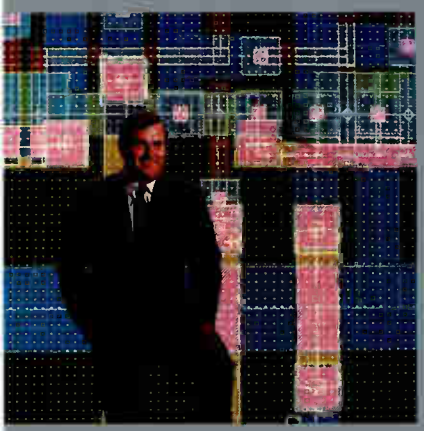

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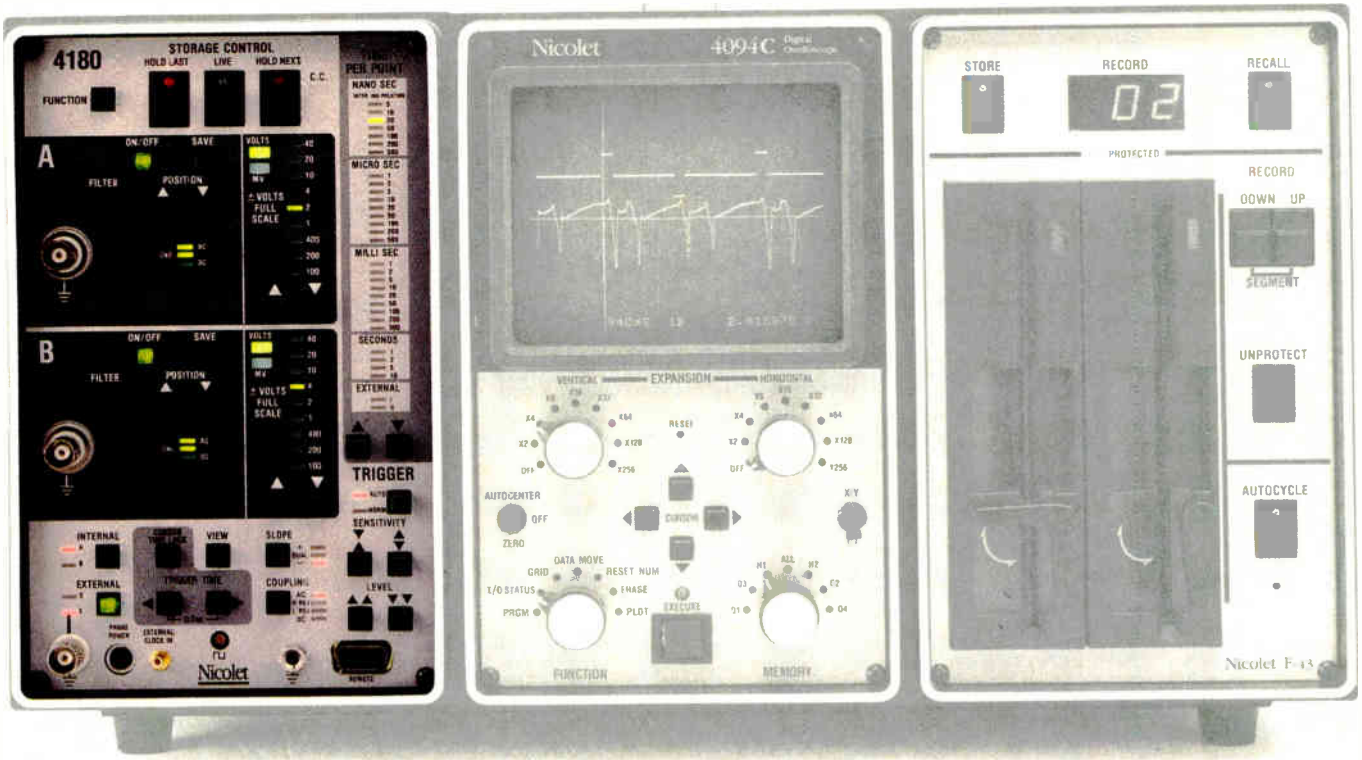

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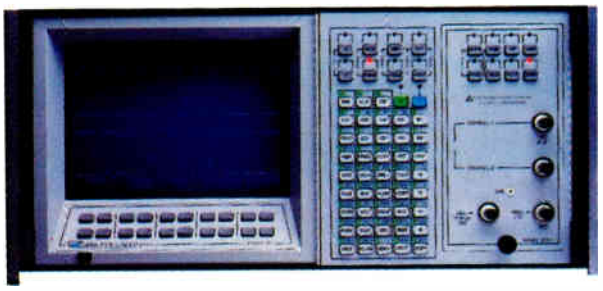

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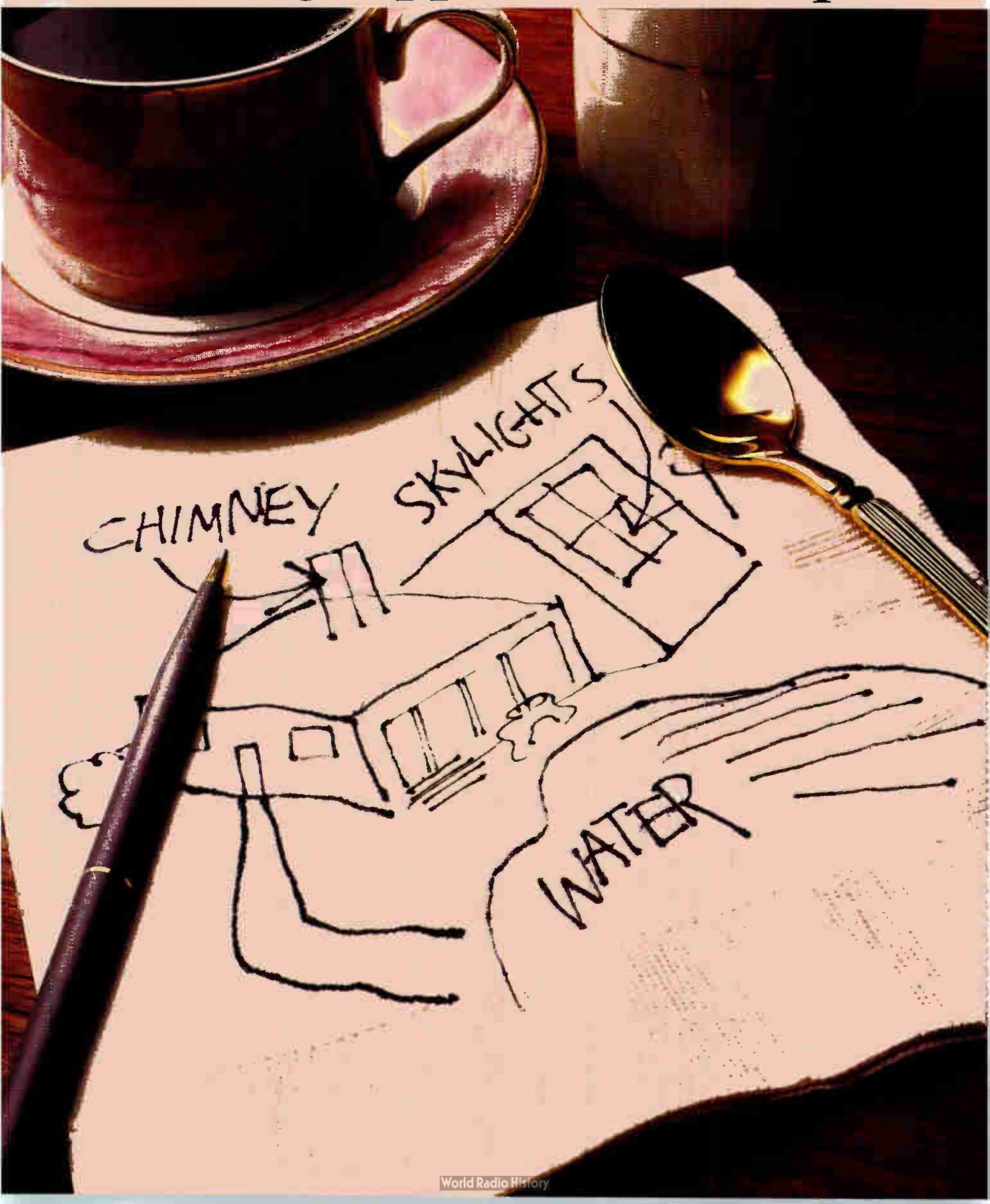

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Q. Medical systems and equipment
R. Industrial control systems and equipment
G. Semiconductor production equipment (component insertion, coil winding, etc.)
H. Electronic sub-assemblies, components and materials (active and passive components, ICs, discretes, hybrids, power supplies)
I. Other manufacturers using electronic equipment as part of their manufacturing process (machine tools, chemicals, metals, plastics, pharmaceuticals, etc.)
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L. Research and development organizations which are part of an educational institution
M. Independent software developers
N. Operators of communications equipment (utilities, railroads, police, airlines, broadcasters, etc.)
O. Educational: 2-4 year colleges, universities
P. Other (please describe)

2. ☐ Your principal job function: (Insert one code only)

A. Corporate management (owner, partner, president, VP, etc.)
B. Operating management (general manager, group manager, division head, etc.)
C. Engineering management (project manager, chief engineer, section head, VP of engineering, VP of research and development, VP of quality control, etc.)
D. Software engineering
E. Systems engineering/integration
F. Quality control engineering (reliability and standards)
G. Design engineering
H. Engineering support (lab assistant, etc.)
I. Test engineering (materials, test, evaluation)
J. Field service engineering
K. Research and development (scientist, chemist, physicist, etc.)
L. Manufacturing and production
M. Purchasing and procurement
N. Marketing and sales
O. Professor/instructor at
P. Senior student at
Q. Graduate student at
Z. Other (please describe)

3. ☐ Your principal responsibility: (Insert one code only)

1. General management
2. Engineering management
3. Engineering
4. Other

4. Estimated number of employees at your location: (Check one box only)

☐ 1 to 49 ☐ 50 to 249 ☐ 250 to 999 ☐ 1,000 or more

5. Your engineering function: (Check all that apply)

A. ☐ I design or develop electronic products and systems (hardware and/or software)
B. ☐ I supervise electronic design or development engineering work
C. ☐ I set standards for, evaluate, test and/or support the manufacture of design components, systems and materials
D. ☐ Other function (please describe)

6. In your company or organization, do you participate in: (Check all that apply)

A. ☐ Business planning and forecasting
B. ☐ Product planning
C. ☐ Technology planning
D. ☐ No involvement in planning

7. Your involvement in the following stages of product development: (Check all that apply)

A. ☐ Evaluate the need for new products
B. ☐ Develop device specifications
C. ☐ Evaluate suppliers
D. ☐ Review prices and availability
E. ☐ Select Vendors
F. ☐ Approve purchases
G. ☐ Place orders
H. ☐ No involvement

8. ☐ What is your title? (Insert one code only)

Operations Management

01. President/Chairman/Owner/Partner
02. Vice President
03. Vice President of Engineering
04. Product Marketing Manager

Engineering Management

11. Technical Director
12. Chief Engineer
13. Principal Engineer
14. Research Director
15. Section Head
16. Project Engineer
17. Senior Engineer
18. Software Manager
19. Senior Test Engineer
20. Senior Field Test Engineer
21. Manufacturing/Production Manager
22. Group Leader
23. Department Head
24. Other Management (please explain)

Design or Standards Personnel

31. Systems Engineer
32. Software Engineer
33. Test Engineer
34. Field Test Engineer
35. Manufacturing Engineer
36. Production Engineer
37. Engineer
38. MTS
39. Consultant
40. Scientist
41. Physicist
42. Other Staff (please explain)

9. Products that you specify or authorize purchase of: (Check all that apply)

ICs and Semiconductors

01. ☐ Digital ICs
02. ☐ Linear ICs
03. ☐ Microprocessors
04. ☐ Semiconductor memories
05. ☐ Custom/semicustom ICs

Components

11. ☐ Resistors and capacitors
12. ☐ Interconnections
13. ☐ Switches and relays
14. ☐ Optoelectronic components
15. ☐ Readout and display devices
16. ☐ Fiber-optic components
17. ☐ Printed circuits

Equipment

21. ☐ Power supplies
22. ☐ Test and measurement equipment
23. ☐ Automatic test equipment
24. ☐ Field service test equipment
25. ☐ Analog/digital panel meters
26. ☐ Cabinets and enclosures
27. ☐ Semiconductor production equipment
28. ☐ Robotics components/equipment
29. ☐ Microprocessor development systems

Computer-based Systems and equipment

31. ☐ CAE hardware/software
32. ☐ CAD/CAM hardware/software
33. ☐ Minicomputers
34. ☐ Microcomputers
35. ☐ Computer terminals
36. ☐ Computer boards
37. ☐ Disk/tape memories
38. ☐ Graphic displays
39. ☐ Software packages/services
40. ☐ Printers/plotters
41. ☐ Computer peripherals
42. ☐ Modems
43. ☐ Communications equipment
44. ☐ None of the above

10. Your degree of profit accountability: (Check one box only)

A. ☐ I have direct profit responsibility
B. ☐ I share profit responsibility with others
C. ☐ I have no profit responsibility

11. Your level of sign-off or purchase approval authority for your company o organization: (Check one box only)

A. ☐ None
B. ☐ Less than $1,000
C. ☐ $1,001 to $ 5,000
D. ☐ $5,001 to $10,000
E. ☐ $10,001 to $25,000
F. ☐ More than $25,000

12. Other publications that you read regularly (3 out of 4 issues): (Check all that apply)

A. ☐ Electronic Design
B. ☐ Electronic Engineering Times
C. ☐ EDN
D. ☐ Electronic News
E. ☐ Electronic Business
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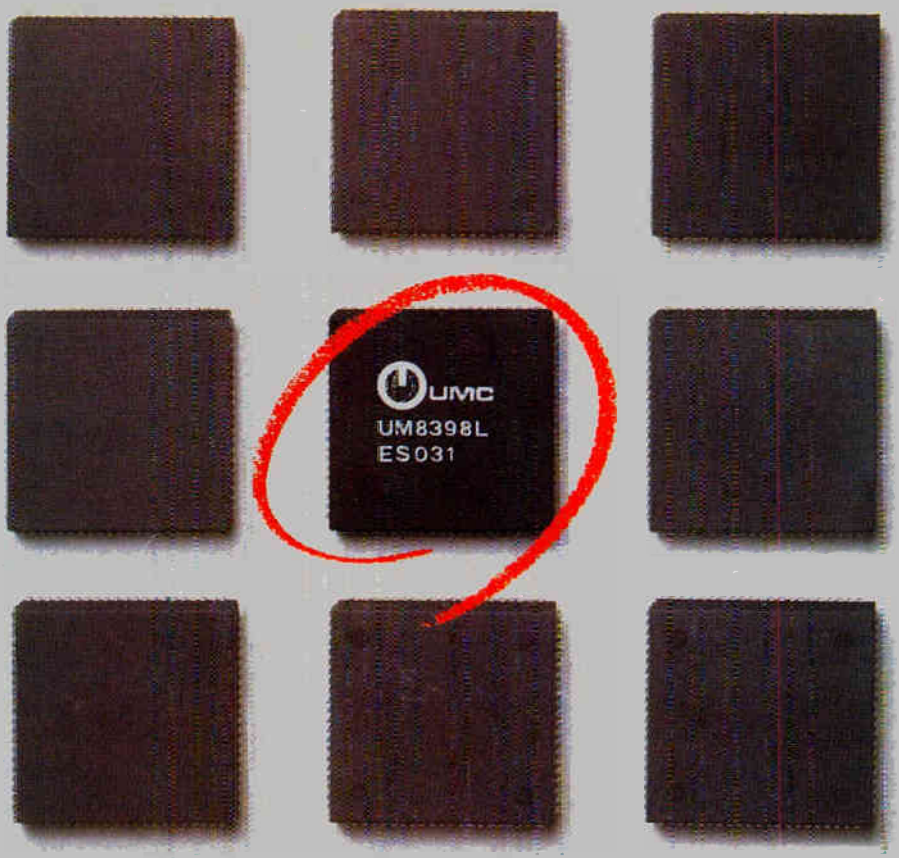

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Circle 47 on reader service card

World Radio History

The ACL Computer Age.

The future belongs to computers and peripherals built with RCA Advanced CMOS Logic (ACL).

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In addition, ACL offers balanced propagation delay, superior input characteristics, improved output source current, low ground bounce and a wider operating supply voltage range.

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*FAST is a trademark of Fairchild Semiconductor Corp.

In Europe, call: Brussels, (02) 246-21-11; Paris, (1) 39-46-57-99; London, (276) 68-59-11; Milano, (2) 82-291; Munich, (089) 63813-0; Stockholm (08) 793-9500.

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Circle 51 on reader service card

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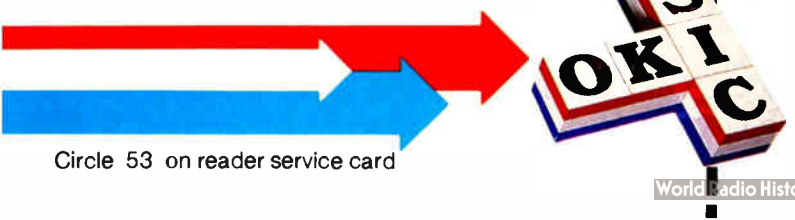

Circle 53 on reader service card

World Radio History

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Other technologically related displays:
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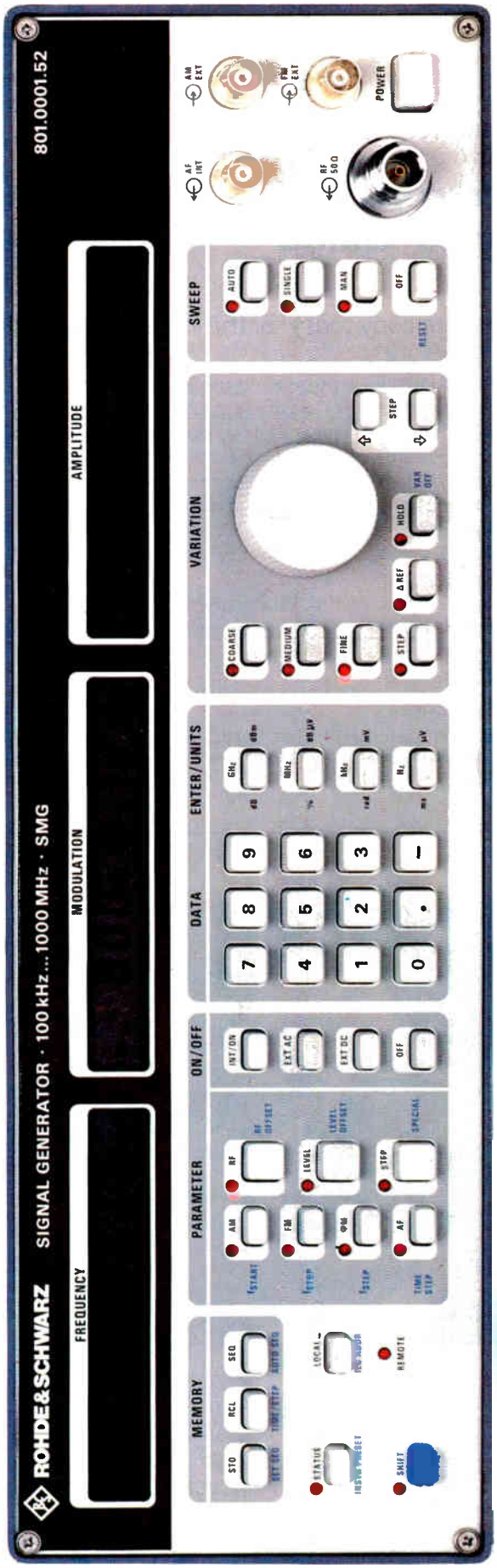
World Radio History

Signal Generator SMG



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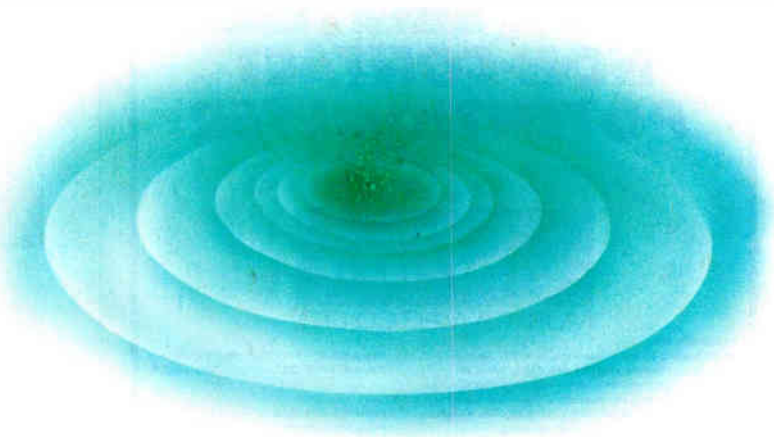

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Circle 119 on reader service card.

World Radio History

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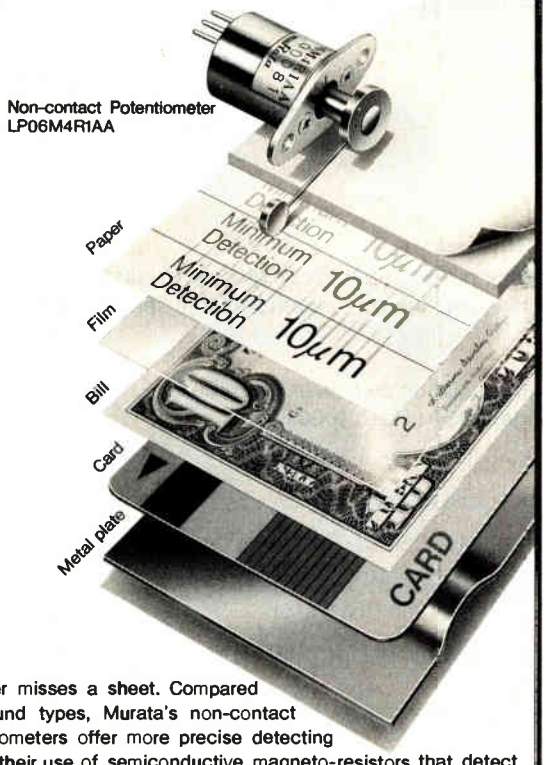
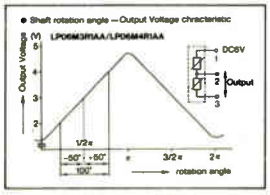
Exact Thickness Detection



It never misses a sheet. Compared to wound types, Murata's non-contact potentiometers offer more precise detecting due to their use of semiconductive magneto-resistors that detect the position of objects at rest or in motion.The ability to detect without physical contact makes them more reliable, and their small size makes them excellent for size reduction. To meet the need for sensors that perfectly detect the thickness of paper, film, cards, currency and other objects, call your nearest Murata office.



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THE 1987/88

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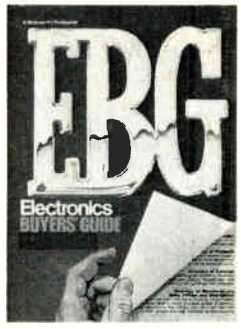

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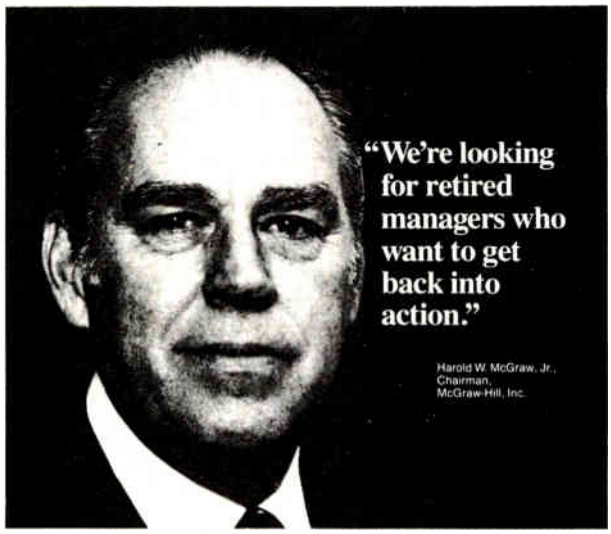

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World Radio History

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	MAX CURRENT AT AMBIENT OF (A) 40°C	50°C	60°C	DIMENSIONS (inches)	PRICE QTY. 1	QTY. 100	QTY. 250	QTY. 1000	MODEL
5V ±5% ADJ.	2.0	2.0	1.00	1.22 × 2.91 × 2.83	$ 43.00	$ 34.50	$ 25.75	$ 22.75	**LSS-34-5**
	3.0	3.0	1.50	1.42 × 2.91 × 3.35	51.00	44.25	30.50	28.00	**LSS-35-5**
	5.0	5.0	2.50	1.54 × 2.91 × 4.13	79.00	60.00	47.50	37.50	**LSS-36-5**
	10.0	10.0	5.00	1.54 × 3.74 × 4.72	106.00	88.00	63.50	58.25	**LSS-37-5**
	20.0	20.0	10.00	2.17 × 3.74 × 6.30	150.00	135.00	104.00	94.50	**LSS-38-5**
	30.0	30.0	15.00	2.56 × 3.74 × 7.09	215.00	165.00	141.00	129.00	**LSS-39-5**
6V ±5% ADJ.	1.7	1.7	0.85	1.22 × 2.91 × 2.83	43.00	34.50	25.75	22.75	**LSS-34-6**
	2.5	2.5	1.25	1.42 × 2.91 × 3.35	51.00	44.25	30.50	28.00	**LSS-35-6**
	4.2	4.2	2.10	1.54 × 2.91 × 4.13	79.00	60.00	47.50	37.50	**LSS-36-6**
	8.4	8.4	4.20	1.54 × 3.74 × 4.72	106.00	88.00	63.50	58.25	**LSS-37-6**
	17.0	17.0	8.50	2.17 × 3.74 × 6.30	150.00	135.00	104.00	94.50	**LSS-38-6**
	25.5	25.5	12.50	2.56 × 3.74 × 7.09	215.00	165.00	141.00	129.00	**LSS-39-6**
12V ±5% ADJ.	0.9	0.9	0.45	1.22 × 2.91 × 2.83	43.00	34.50	25.75	22.75	**LSS-34-12**
	1.3	1.3	0.65	1.42 × 2.91 × 3.35	51.00	44.25	30.50	28.00	**LSS-35-12**
	2.1	2.1	1.05	1.54 × 2.91 × 4.13	79.00	60.00	47.50	37.50	**LSS-36-12**
	4.2	4.2	2.10	1.54 × 3.74 × 4.72	106.00	88.00	63.50	58.25	**LSS-37-12**
	8.5	8.5	4.25	2.17 × 3.74 × 6.30	150.00	135.00	104.00	94.50	**LSS-38-12**
	12.5	12.5	6.25	2.56 × 3.74 × 7.09	215.00	165.00	141.00	129.00	**LSS-39-12**
15V ±5% ADJ.	0.7	0.7	0.35	1.22 × 2.91 × 2.83	43.00	34.50	25.75	22.75	**LSS-34-15**
	1.0	1.0	0.50	1.42 × 2.91 × 3.35	51.00	44.25	30.50	28.00	**LSS-35-15**
	1.7	1.7	0.85	1.54 × 2.91 × 4.13	79.00	60.00	47.50	37.50	**LSS-36-15**
	3.4	3.4	1.70	1.54 × 3.74 × 4.72	106.00	88.00	63.50	58.25	**LSS-37-15**
	7.0	7.0	3.50	2.17 × 3.74 × 6.30	150.00	135.00	104.00	94.50	**LSS-38-15**
	10.0	10.0	5.00	2.56 × 3.74 × 7.09	215.00	165.00	141.00	129.00	**LSS-39-15**
24V ±5% ADJ.	0.5	0.5	0.25	1.22 × 2.91 × 2.83	43.00	34.50	25.75	22.75	**LSS-34-24**
	0.7	0.7	0.35	1.42 × 2.91 × 3.35	51.00	44.25	30.50	28.00	**LSS-35-24**
	1.1	1.1	0.55	1.54 × 2.91 × 4.13	79.00	60.00	47.50	37.50	**LSS-36-24**
	2.1	2.1	1.05	1.54 × 3.74 × 4.72	106.00	88.00	63.50	58.25	**LSS-37-24**
	4.5	4.5	2.25	2.17 × 3.74 × 6.30	150.00	135.00	104.00	94.50	**LSS-38-24**
	6.5	6.5	3.25	2.56 × 3.74 × 7.09	215.00	165.00	141.00	129.00	**LSS-39-24**
28V ±5% ADJ.	0.4	0.4	0.20	1.22 × 2.91 × 2.83	43.00	34.50	25.75	22.75	**LSS-34-28**
	0.6	0.6	0.30	1.42 × 2.91 × 3.35	51.00	44.25	30.50	28.00	**LSS-35-28**
	0.9	0.9	0.45	1.54 × 2.91 × 4.13	79.00	60.00	47.50	37.50	**LSS-36-28**
	1.8	1.8	0.90	1.54 × 3.74 × 4.72	106.00	88.00	63.50	58.25	**LSS-37-28**
	3.8	3.8	1.90	2.17 × 3.74 × 6.30	150.00	135.00	104.00	94.50	**LSS-38-28**
	5.5	5.5	2.75	2.56 × 3.74 × 7.09	215.00	165.00	141.00	129.00	**LSS-39-28**
48V ±5% ADJ.	0.2	0.2	0.10	1.22 × 2.91 × 2.83	43.00	34.50	25.75	22.75	**LSS-34-48**
	0.3	0.3	0.15	1.42 × 2.91 × 3.35	51.00	44.25	30.50	28.00	**LSS-35-48**
	0.5	0.5	0.25	1.54 × 2.91 × 4.13	79.00	60.00	47.50	37.50	**LSS-36-48**

Triple Output.

	VOLT Vo	MAX OUTPUT CURRENT (AMPS) 40°C	50°C	60°C	MAX OUTPUT POWER (WATTS) 40°C	50°C	60°C	DIMENSIONS (inches)	PRICE QTY. 1	QTY. 100	QTY. 250	QTY. 1000	MODEL
$5V^{+0.3}_{-0.3}$ V ADJ., ±12V FIXED	5	7.00	7.00	4.55	50	50	32.5	1.42 × 3.74 × 6.10	$118.00	$ 84.00	$ 71.00	$ 66.00	**LST-37-133**
	+12	1.50	1.50	0.97									
	−12	0.50	0.50	0.32									
	5	8.00	8.00	5.20	76	76	49.4	1.61 × 3.74 × 6.89	146.00	108.00	95.00	86.00	**LST-38-133**
	+12	3.20	3.20	2.00									
	−12	0.50	0.50	0.32									
	5	13.00	13.00	8.45	101	101	65.6	1.93 × 3.74 × 7.48	169.00	129.00	117.00	106.00	**LST-39-133**
	+12	4.00	4.00	2.60									
	−12	1.00	1.00	0.65									
$5V^{+0.3}_{-0.3}$ V ADJ., ±15V FIXED	5	7.00	7.00	4.55	50	50	32.5	1.42 × 3.74 × 6.10	118.00	84.00	71.00	66.00	**LST-37-144**
	+15	1.20	1.20	0.78									
	−15	0.50	0.50	0.32									
	5	8.00	8.00	5.20	75	75	49.0	1.61 × 3.74 × 6.89	146.00	108.00	95.00	86.00	**LST-38-144**
	+15	2.50	2.50	1.60									
	−15	0.50	0.50	0.32									
	5	13.00	13.00	8.45	103	103	67.0	1.93 × 3.74 × 7.48	169.00	129.00	117.00	106.00	**LST-39-144**
	+15	3.20	3.20	2.00									
	−15	1.00	1.00	0.65									
$5V^{+0.3}_{-0.3}$V ADJ., +12V −5V FIXED	5	7.00	7.00	4.55	50	50	32.5	1.42 × 3.74 × 6.10	118.00	84.00	71.00	66.00	**LST-37-131**
	+12	1.50	1.50	0.97									
	5	0.50	0.50	0.32									
	5	8.00	8.00	5.20	725	725	46.5	1.61 × 3.74 × 6.89	146.00	108.00	95.00	86.00	**LST-38-131**
	+12	3.20	3.20	2.00									
	5	0.50	0.50	0.32									
	5	13.00	13.00	8.45	94	94	61.0	1.93 × 3.74 × 6.89	169.00	129.00	117.00	106.00	**LST-39-131**
	+12	4.00	4.00	2.60									
	5	1.00	1.00	0.65									

World Radio History

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REGULATED VOLTAGE

regulation, line ..... 0.4% for input variations from 85 to 132VAC or 132 to 85VAC.

regulation, load ..... 0.8% for load changes from zero to full load and from full load to zero on LSS models. 0.8% for load changes from .75A to full load on main output of LST-37; from 1.5A to full load on main output of LST-38, LST-39. 150mV max from zero to full load and full load to zero on auxiliary outputs of LST-37, 38, 39 with main output preloaded.

ripple and noise. ..... 15mV RMS for all models; 120mV pk-pk for 5V and 6V models; 150mV pk-pk for 12V and 15V models; 200mV pk-pk for 24V and 28V models.

temperature coefficient ..... 0.02%/°C.

AC INPUT
line ..... 85 to 132VAC, 47-440Hz.

DC INPUT
110 to 175VDC.

EFFICIENCY
72% typical for 5V LSS models. 70% typical for LST models, and 12V and 15V LSS models. 82% typical on 24V through 48V LSS models.

OVERSHOOT
No overshoot at turn-on, turn-off or power failure.

OPERATING TEMPERATURE RANGE
0-60°C with suitable derating above 50°C.

STORAGE TEMPERATURE RANGE
−30°C to +85°C.

OVERLOAD PROTECTION
External overload protection, automatic electronic current limiting circuit, limits output current to a safe, preset value, thereby protecting the load as well as the power supply.

OVERVOLTAGE PROTECTION
Overvoltage protection is standard on all LSS models and on main output of LST Models. If output voltage increases above a preset level, inverter drive is removed.

HOLD UP TIME
5V and 6V LSS models, and all LST models will remain within regulation limits for at least 16.7 msec. after loss of AC power when operating at full load, nominal output voltage and 100VAC input voltage.

IN-RUSH CURRENT LIMITING
The turn-on in-rush current will not exceed 15A typical on LSS-38, LSS-39; 24A typical for LSS-34; 30A typical for LSS-35, LSS-36, LSS-37; 15A typical for LST-38, LST-39; 35A typical on LST-37.

COOLING
Convection cooled, no fans or blowers needed.

DC OUTPUT CONTROLS
Simple screwdriver adjustment.

REMOTE SENSING
Provision is made for remote sensing to eliminate the effects of power output lead resistance on DC regulation for LSS-38 and LSS-39.

INPUT AND OUTPUT CONNECTIONS
All input and output connections are made via barrier strip terminals.

OUTPUT STATUS INDICATOR
LED indicates presence of output voltage on LSS models and 5V output of LST models.

MOUNTING
Two mounting surfaces, two mounting positions. One mounting surface and one mounting position for LSS-39. Some derating may be required in horizontal mounting position.

ISOLATION RATING
2000V RMS input to output.

PHYSICAL DATA

Package Model	Weight Lbs. Net	Weight Lbs. Ship	Size Inches
LSS-34	0.46	0.55	1.22 × 2.91 × 2.83
LSS-35	0.64	0.75	1.42 × 2.91 × 3.35
LSS-36	0.66	0.75	1.54 × 2.91 × 4.13
LSS-37	0.88	1.00	1.54 × 3.74 × 4.72
LST-37	0.93	1.10	1.42 × 3.74 × 6.10
LST-38	1.21	1.41	1.61 × 3.74 × 6.89
LST-39	1.54	1.79	1.93 × 3.74 × 7.48
LSS-38	1.54	1.85	2.17 × 3.74 × 6.30
LSS-39	2.31	2.50	2.56 × 3.74 × 7.09

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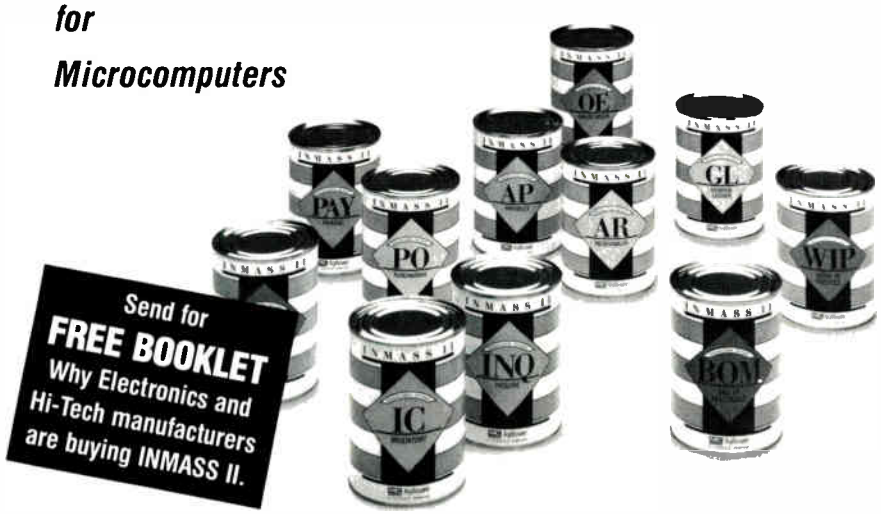

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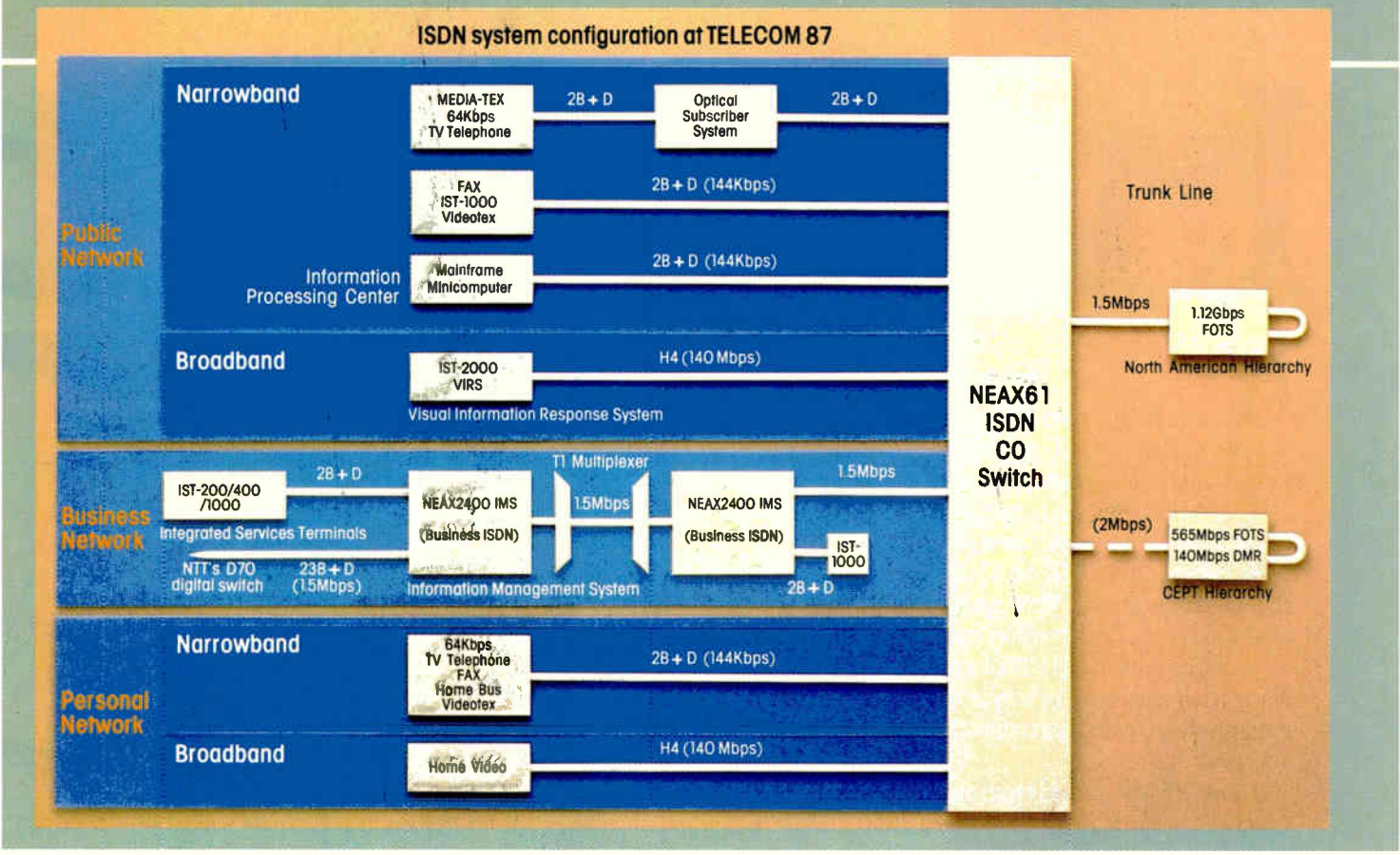

Digital switching system: NEAX61

The core of the demonstration was the NEAX61. It displayed integrated broad- and narrowband switching capability, as well as 1.5Mbps high-speed packet switching.

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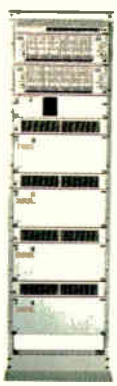
The NMS efficiently monitors/controls switching and transmission networks. For easy trouble-shooting, it offers expert system technology which guides users to the source of system problems.

1.12Gbps FOTS

The 1.12Gbps Fiber Optic Transmission System (FOTS) demonstrated its ability to combine 16,128 voice channels into a single-mode fiber.



AT THE R&D ZONE

NEC's intensive R&D efforts, ranging from components to total systems, gave visitors a glimpse of many futuristic visions come true.

4Gbps FOTS

This ultra high-speed system utilizes 1.55μm DFB LDs and InGaAs APDs and transmits over 30km without repeaters.

Photonic switching

NEC's display included a photonic switching system with 8×8 matrix optical switches. The system demonstrated 140Mbps broadband switching capability using IST-2000 video communication terminals.

High resolution CCD color camera

A compact HDTV camera, featuring 1.24-million pixel CCD chips, showed the latest advance in CCD technology.

NEC

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WHY VTC? ASK THE VME CONSORTIUM.

"For a bunch of companies that don't always agree on everything, we sure were unanimous on VTC."

The VME Consortium needed an economical, yet highly functional VME bus interface chip, to minimize design time . . . and to help raise the VME standard to higher levels.

"We looked at the leading suppliers," said Joe Ramunni, consortium chairman (and president of Mizar), "and VTC came out on top. Their CMOS standard-cell ASIC approach gave us the high drive capability we needed, optimized for bus interfacing. And, it proved much more cost-effective, with higher performance, than gate array technology."

The VME Consortium is made up of such firms as Plessey Microsystems, Omnibyte Corporation, Mizar Inc., Ironics Inc., Heurikon Corporation, Matrix Corporation, and Clearpoint Inc., among others. What did they look for in a supplier?

"We needed a credible business partner," said Ramunni, "with a proven track record, who could provide a turnkey package . . . both design and fab. A supplier that could produce in quantity, and provide technical support to the market at large.

"We also needed a firm with an international marketing structure, because we expect this chip to be the de facto standard worldwide.

"But, we needed *people* we could work with, too. VTC had the right 'comfort factor'."

Jack Regula, consortium technical director (and VP-R&D, Ironics) added: "Our requirements for high speed, high gate-count, low power consumption, and VME bus drive capability were all met well with VTC's 1-micron CMOS standard cell library. And we were extremely impressed with VTC's facilities, its people, and its customer list."

In the future, the VME bus chip (VIC) will become a standard cell within VTC's CMOS library, to allow customers to further customize the chip.

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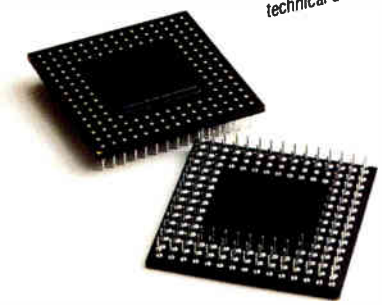
Joseph Ramunni, chairman (left), and Jack Regula, technical director, VME Technology Consortium.



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INSIDE TECHNOLOGY

A TORRENT OF FUTURE PRODUCTS AT THE SOLID STATE CONFERENCE

Now more than ever, the ISSCC is the leading barometer for divining the future direction of the semiconductor industry and its customers; the annual event is clearly the center stage for previewing significant upcoming products

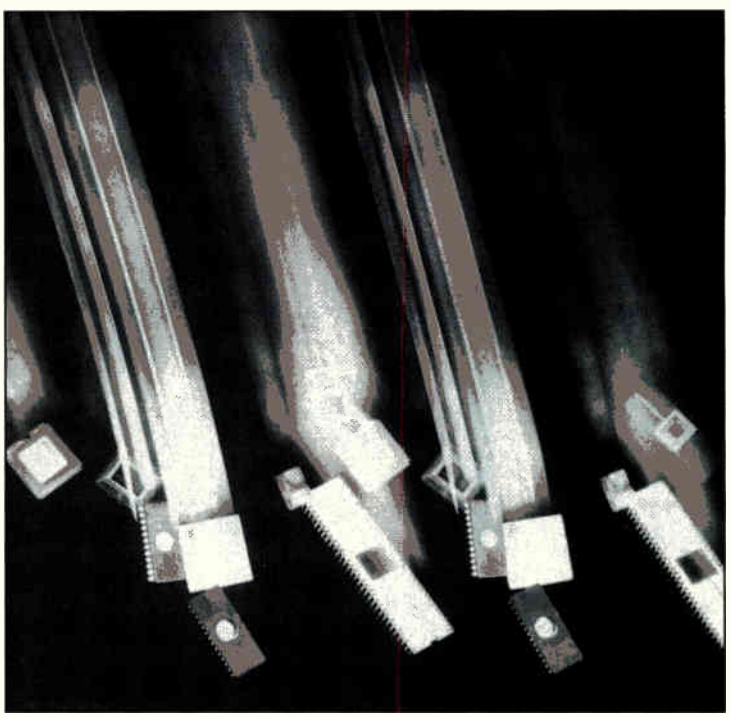
by Bernard C. Cole

The annual International Solid State Circuits Conference, convening in San Francisco this week, looks like the best one yet. More than ever, the 31-year-old conference is turning into the leading barometer for reading the future direction of the semiconductor industry and its systems customers. Not only does the ISSCC continue to be the premier forum for reporting on new technology, but it is now the stage on which chip makers preview major new products slated for introduction anytime from the next few months to the next two years. This year's incredibly rich harvest of papers points to the following new products:

- A flood of various memories that push the frontier of density and speed. This year, papers from Hitachi, Matsushita, and Toshiba report on 16-Mbit dynamic random-access-memory designs (see p. 68). Equally impressive are the high-density, high-speed static RAMs, including sub-35-ns 1-Mbit circuits from Fujitsu, Hitachi, IBM, Mitsubishi, and Philips (see p. 69), as well as sub-15-ns ECL-compatible biCMOS SRAMs from Hitachi, Fujitsu, National Semiconductor, and Texas Instruments (see p. 71). These devices make it possible for system designers to rethink the hierarchy of memory storage. For example, 16-Mbit dynamic RAMs mean replacing several megabytes of disk drive with a single circuit. And sub-50-ns static RAMs in the 1-Mbit range can be substituted for dynamic RAMs in the main memory of many 32-bit microprocessor-based applications.
- A slew of specialized application- and algorithm-specific processors performing functions previously handled in software. One particular focus this year is graphics, with specialized processors from General Electric, Matsushita, Nippon Telegraph & Telephone Corp., Toshiba, and Visual Information Technologies (see p.73).
- A host of analog-to-digital-converter chips (see p. 77) that show there is more than one way to get high speed, accuracy, and resolution.

Along with the general trends are the individual achievements. These include:

- Intel Corp.'s introduction of a 4-Mbit ultraviolet-erasable programmable read-only memory. It opens numerous new application areas (see p. 72). A single nonvolatile memory chip will be able to store as much data as several floppy disks.
- Rockwell International's 8-bit-slice, 1-μm depletion MES FET gallium arsenide processor. As well as reaching an impressive level of complexity for GaAs, it runs at 150 million operations per second (see p. 74).
- Actel Corp.'s antifuse-based configurable gate arrays. They could combine the density of traditional gate arrays with the flexibility of EPROM and EEPROM-based programmable logic devices (see p. 75).
- The source of many future chips will be IBM's computer-aided-design system, which is capable of designing chips with a mixture of analog and digital devices and standard cells that have 75% routability. It uses a maze-runner algorithm to generate wiring automatically (see p.76).



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THE NEXT WAVE: 16-MBIT DRAMS FROM JAPAN

An announcement concerning dynamic random-access memories at the ISSCC in recent years has almost always had the ability to astound, often leaving attendees shaking their heads in amazement and, in the case of U.S. engineers, not a little regret and perplexity. This year's meeting in San Francisco is no exception.

Scarcely has production begun on 1-Mbit DRAMs and approached the sampling stage on a few 4-Mbit circuits than the 16-Mbit DRAM is on the scene—not from one source, but from three. And all of them are Japanese. Hitachi Ltd. is showing a 16-Mbit design employing a transposed data-line structure; Matsushita Electric Industrial Co.'s device has an open-bit-line architecture; and Toshiba Corp. is demonstrating a unique design that incorporates a serial 1-Mbit high-speed read/write mode.

When these devices are finally brought to the marketplace, advanced 16- and 32-bit microprocessors will finally have a memory device to match their megabytes of address space. In terms of system performance, a typical personal computer with such high-density DRAMs could achieve as much as a tenfold improvement in performance, due to the fact that half a dozen of the most memory-hungry application programs for word processing, spreadsheets, and desktop publishing could be located in DRAM. This means they would not need to be constantly seeking to access the disk drives.

But if the efforts described so far by these three companies are any indication, there are considerable technical hurdles left to overcome. It will be at least 1990 before such devices begin appearing in sample quantities.

At Hitachi, engineers have come up with a single 5-V design with an internal 3.3-V operating voltage for the memory array. This design allows access times in the 60-ns range and cycle times of about 180 ns, with a typical power dissipation of 420 mW. To get such performance, Hitachi designers have gone to a 0.6-μm twin-well CMOS process using double-level metal.

One of the major problems the Hitachi designers have run into is interference noise due to an increase in interdata-line capacitance. Although similar problems have occurred at lower densities, at the 16-Mbit level they take on new importance. The engineers report encountering a new form of data-line interference noise generated during the sense-amplifier operation. It was to address this problem that they devised their transposed data-line structure, which should reduce such noise by a factor of about three—from roughly 25% of the signal to less than 10%.

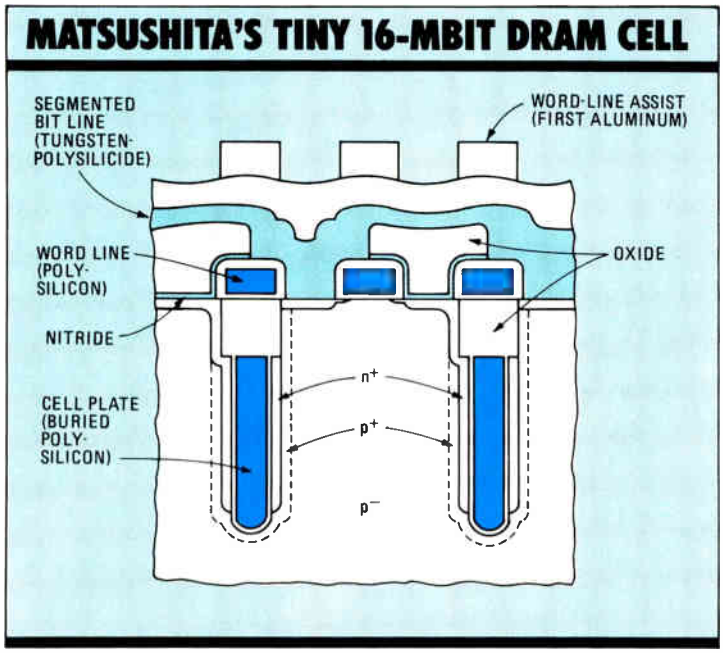
BRINGING DOWN THE SIZE

The designers at Matsushita have posed themselves an even more difficult problem, a 16-Mbit design with roughly the same access and cycle times as the Hitachi device, but tucked into a diminutive chip area. The Matsushita designers have been able to build a cell with an area of 4 μm^2, which allows the DRAM to be incorporated into a low-cost, 300-mil, dual in-line package. To shrink the cell, Matsushita uses a 0.5-μm n-well CMOS process with double polysilicon, double metal, and a single level of polysilicide (see figure).

The traditional open-bit-line architecture and trench isolation that Matsushita uses make possible the small-geometry cell. But the total packing density is constrained, since scaling of the cell is limited by the layout pitch of the array's sense amplifiers. To reduce the size of the total array, the designers devised a relaxed sense-amplifier pitch scheme.

The only problem with this modified open-bit-line architecture, in common with earlier designs, is that it still has a noise immunity far inferior to the less dense folded-bit-line approach. So, the designers have adopted a reverse dummy word-line technique for use in a memory array segmented into thirty-three 512-Kbit blocks of 2,048 segmented bit lines and 256 word lines.

In this design, one reverse dummy word line is assigned to each 256 word-line segment. Only a dummy word line belonging to the segment having an accessed word line turns to a low level;



Matsushita achieves minimum cell size in its open-bit-line architecture using a trench construction for the storage capacitor.

World Radio History

the other dummy word lines of nonselected segments are kept high. Consequently, the researchers say, the noise that occurs by coupling between the word line and the bit line is canceled.

The Toshiba 70-ns DRAM achieves 16-Mbit density through a combination of advanced CMOS processing, a new stacked trenched-capacitor cell, and a pseudo-open-bit-line layout. Using 0.7-μm design rules, the device incorporates a cell measuring 6.12 μm^2 and fabricated using a p-well CMOS process with three levels of polysilicon, two levels of aluminum, and a single level of molybdenum silicide. Intended for applications in high-definition image processing, the RAM has been developed to have a 100-MHz serial read/write mode for up to 2 Kbits of continuous data.

The peripheral circuits are formed with a twin-tub CMOS process. As in the other 16-Mbit designs, the device employs a trenched capacitor cell. But to reduce intercell leakage, the memory cell is constructed with a polysilicon-to-polysilicon capacitor in a trench and a side-wall diffusion layer from the first layer of polysilicon.

To increase packing density, designers at the company's VLSI Research Division in Kawasaki use a pseudo-open-bit-line architecture. In this architecture, blocks of 32-bit columns are laid out alternately as open-bit and folded-bit-line arrays. Since the polysilicon cell plate is located below, rather than beside, the switching transistor, self-aligning contacts are not needed to connect the bit line to the cell. In order to save space in the area devoted to decode logic, the second aluminum is used for column-select lines from a common column decoder.

–Bernard C. Cole

TECHNOLOGY TO WATCH is a regular feature of *Electronics* that provides readers with exclusive, in-depth reports on important technical innovations from companies around the world. It covers significant technology, processes, and developments

TECHNOLOGY TO WATCH **ISSCC**

FIVE BLAZING FAST CMOS SRAMS ARE COMING

As eye-catching as the 16-Mbit dynamic random-access memories may be, the development that will have a more immediate effect on the way memory is implemented is the new breed of static RAMs combining 1-Mbit density with blazing speed. Five such CMOS devices—three from Japan and one each from the U. S. and the Netherlands—emerged at this year's ISSCC boasting access times ranging from 14 to 30 ns. The entries come from Japan's Fujitsu Ltd., Hitachi Ltd., and Mitsubishi Electric Corp., as well as from IBM Corp.'s General Technology Division in Essex Junction, Vt., and Philips's Research Laboratories in Eindhoven, the Netherlands.

Other than using CMOS as the base process, the five SRAMs have little in common. Four designs—from IBM, Hitachi, Mitsubishi, and Philips—are built around a six-transistor cell for high speed. Fujitsu Ltd. has instead opted for a four-transistor design with polysilicon resistor loads to achieve high density. The Philips chip is organized as 128 K by 8 bits, while those from Fujitsu and Hitachi feature a 256-K-by-4-bit architecture. The IBM SRAM can be configured by laser personalization into 128 K by 8 bit, 256 K by 4 bit, or 1 M by 1 bit. The Mitsubishi chip boasts a 1-M-by-1-bit organization, dynamically reconfigurable for testing to 256 K by 4 bits.

Once such high-speed 1-Mbit SRAMs become commercially available in the next year or so, designers of personal computers and low-end work stations using 32-bit complex- or reduced-instruction-set central processing units will have to rethink the way they use memory, says the chairman of the SRAM session at the ISSCC. "Currently available 32-bit CPUs running at 10 to 20 MHz are far outdistancing the performance of the 70- to 120-ns 256-Kbit and 1-Mbit CMOS DRAMs," says Roger Kung, who is director of MOS memory design at Motorola Inc. in Austin, Texas.

As a result, system designers currently must either employ wait states to compensate for the lower-speed main memory, or incorporate lower-density 15- to 35-ns data-cache and tag-cache SRAMs between the CPU and the higher-density main memory. "With the availablity of 15- to 35-ns 1-Mbit SRAMs, designers who can afford it can build 32-bit-based systems with just one kind of memory device," Kung says. "This will considerably simplify their designs and significantly lower overall system cost."

The most flexible 1-Mbit SRAM design is IBM's. In addition to the three organizations, it can also be configured to run asynchronously, with static-column and chip-enable speed-up modes; or synchronously, with a fast-page or static-column mode. As an asynchronous device, access time is 34 ns. In the static-column mode, access time is 33 ns, and in the chip-select speed-up mode, 29 ns. As a synchronous SRAM, access time is 29 ns, with a fast-page-mode speed of 24 ns.

To achieve a size of about 58 μm^2 for the six-transistor cell, the IBM device uses a 0.9-μm retrograde n-well polysilicon CMOS process with two metal layers, one of tungsten and one of aluminum. Active power dissipation is 225 mW in the synchronous mode and 230 mW in the asynchronous. Consisting of four quadrants of 256 Kbits partitioned into eight blocks of 32 Kbits each, the device has a chip area of 10.8 by 8.5 mm^2. It can operate off either 3.3- or 5-V supplies.

Departing from the six-transistor approach is

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ONE-CHIP ADCs REACH 2 GHz; OTHERS HIT 18-BIT ACCURACY

This year's ISSCC clearly demonstrates why the analog-to-digital converter remains the quintessential analog circuit and why no other function better represents its class. The ADC continues to dazzle with architectural virtuosity that vaults it to unprecedented heights of resolution, speed, and accuracy.

Driven by the needs of video and digital signal processing, among other things, single-chip ADCs are rising to the occasion, reaching sampling rates of 2 GHz and resolutions of 18 bits, albeit not simultaneously. To stretch that far in performance, however, architectural design alone may not be enough, says Robert Blauschild, chairman of the session on ADCs. Indeed, advances in mortar and brick—in the form of advanced processing—are just as essential in some cases.

So, while some designers at the ISSCC are busy describing monoliths wrought with such techniques as pipelining, error correction, sampling-and-holding, recursion, and folding, others are revealing the biCMOS and leading-edge bipolar processes making possible the techniques or contributing to the speed of operation. One unusual converter, to be described by engineers from Analog Devices Inc., Wilmington, Mass., is highly representative of the new breed. Intended for audio-digital-signal processing and designed by both analog and digital experts, the 10-μs device converts its 14 bits in five successive (recursive) passes through a 4-bit flash subconverter, each time narrowing down its range. It accepts its ac input signal through an on-board sample-and-hold amplifier. To do all that, the chip's circuits are carved from biCMOS—CMOS for its complex logic and output registers, bipolar for its sample-and-hold and other amplifiers.

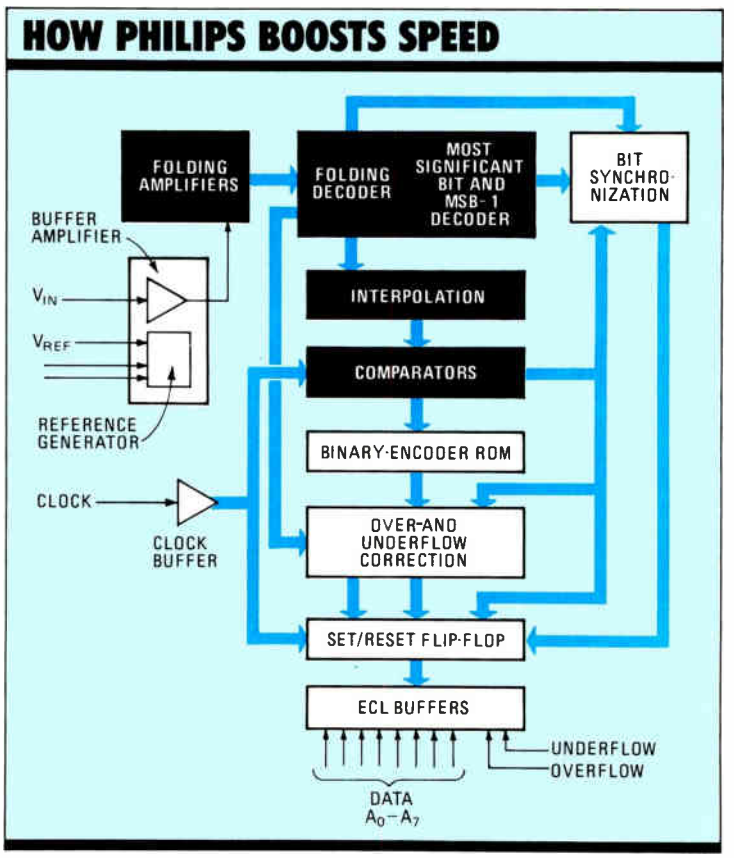
Another high riser, from Philips Research Laboratories in Sunnyvale, Calif., is an 8-bit, 100-MHz flash ADC with a twist—it folds its input signal eight times, interpolates some of the more significant bits, and uses the same comparators a number of times (see figure). The idea is to cut the number of comparators—to 66 from the 255 conventionally needed—and reduce die size so as to realize the stringent signal and clock timing distribution needed to achieve the high speed.

Still another way to get high resolution (above 8 bits) at the speed of flash ADCs—without the attendant hardware—is with pipelining. One chip that does just that comes from the Electronics Research Laboratory at the University of California, Berkeley. According to designers Sehat Ray and Paul Gray, to maintain 13 bits of differential linearity, three stages of pipelining alone were not enough; they had to add a segmented DAC to correct errors. The resulting design could run at 1.5 million samples/s when fabricated in 3-μm CMOS. Instead, the designers chose to optimize for least area. The result: speeds of 250,000 samples/s and dimensions of 1.4 by 1.6 mm.

Pipelining appears again in two other CMOS ADCs. One exhibits high throughput (1 MHz) and linearity (12 bits) with relatively little circuitry. This is achieved by cascading 1-bit ADCs and using a capacitor averaging technique to correct crucial errors. The other strides at 20 MHz and resolves 8 bits by digitally correcting errors and autozeroing its differential comparator/sample-and-hold circuit. The first is a joint effort of the Department of Electrical and Computer Engineering at the University of Illinois in Champaign-Urbana and AT&T Bell Laboratories, Murray Hill, N. J.; the second hails from various groups at Hitachi Ltd. in Tokyo.

Top honors for speed go to Nippon Telegraph and Telephone LSI Laboratories' bipolar flash 6-bit ADC. It samples at a blazing 2 gigasamples/s. Another medal winner, this time for resolution, is an 18-bit performer from NEC Corp. with 105-dB signal-to-noise ratio and 0.003% total harmonic distortion.

–Stan Runyon



Philips cuts the number of comparators in its 8-bit analog-to-digital converter from 255 to 66 in order to reduce die size. The result: 100-MHz flash speed.

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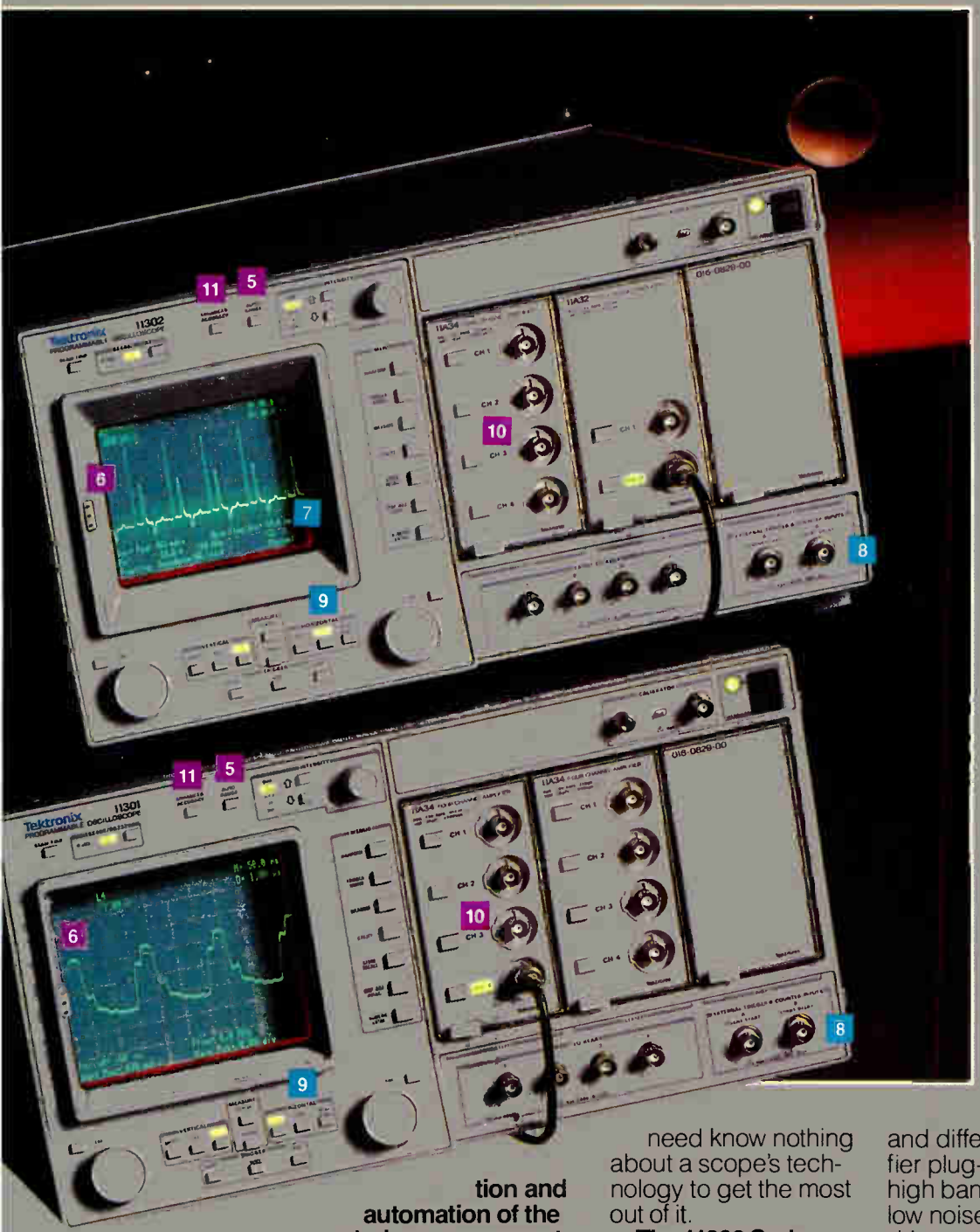

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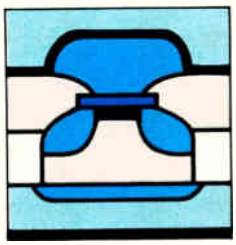


CAN U. S. CHIP PROFITS PAY FOR A NEW GENERATION OF FABS?

The current surge in earnings might make it easier to say yes, but some experts continue to worry that profits over the long term still won't be able to support the high cost of building plants employing the fine-line technology of the 1990s

by J. Robert Lineback

Happy days are here again for the U. S. semiconductor industry, with record profits reported at almost every chip maker, from giants like Intel Corp. down to recent startups. But behind the celebrations, a wide-ranging controversy still rages over the long-term viability of the semiconductor business.

On the one hand, many industry observers are alarmed by the poor long-term return on equity they see among chip makers. Some analysts offer bleak assessments of recent balance-sheet trends and maintain that the low profit margins have set fundamental changes in motion while the industry rode the roller-coaster cycles of the turbulent 1980s. They don't see how industry profits can support the capital-intensive push to the next generation of fine-line chip-fabrication technology.

On the other hand, chip merchants refute the gloom-and-doom scenarios, saying low returns on equity in the 1980s are false profit indicators, warped by the unusually hard times early this decade, notably the punishing market-share wars with Japan. While they worry about the cost of new fab lines, they also see encouraging signs in the market. They feel that careful management, the use of shared foundries, and focused market strategies will pull the industry through.

Such steps are crucial, say most analysts, who put chip-industry returns on equity near a poor 6% average for the decade—about half of what it was in the 1970s and far from the profit margins of most other electronic segments. With that rate of return, they argue, chip makers are not self-supporting.

"They seem to be at a critical crossroad," says Peter Bearse, president of Development Strategies Corp., Gloucester, Mass., which recently conducted an industrywide survey on profit margins for the American Electronics Association. The survey shows chip making second to last in the ratio of net income to equity, when stacked up against other 1987 electronics businesses (see chart, right). And the ratio was lower in the 1987 recovery year than in the weaker 1982 period.

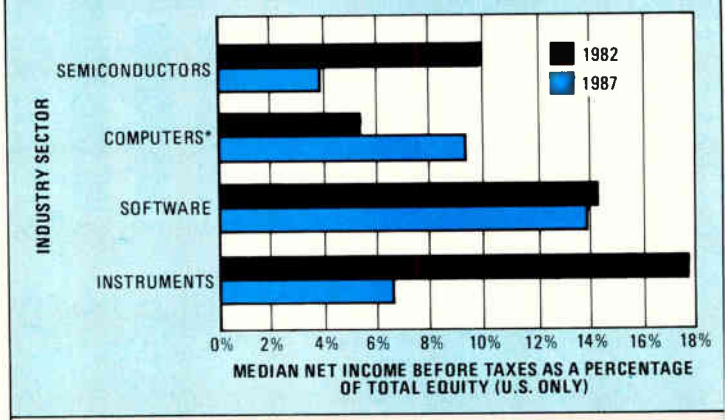
The survey also showed that semiconductor capital expenditure rates were lower than all other major segments except for production equipment (see chart, p. 82). The fast pace of chip technology is quickly making production equipment obsolete, setting up what is expected to be a capital-investment crunch at a time when profit margins are unattractive to investors.

"This is a profitable business, but the long-term problem is that the profits are not enough to pay for the next round of fab," warns analyst Andrew J. Kessler with PaineWebber Inc. in New York.

Michael J. Krasko, managing director at L. F. Rothschild & Co. Inc. in New York agrees. "I think over time it will become increasingly difficult for the semiconductor industry to generate returns that support continued equity investments. The long-term impact is the consolidation of the industry first, and then a greater focus by all semiconductor manufacturers on what areas to pursue."

Chip-company executives respond that the profit declines have been an aberration caused by too

THE FINANCIAL PICTURE IS WORSENING IN THE SEMICONDUCTOR BUSINESS



*NOTE: COMPUTER FIGURES FOR 1982 DO NOT INCLUDE THE THEN-SMALL MICROPROCESSOR-BASED SEGMENT

SOURCES: AMERICAN ELECTRONICS ASSOCIATION AND DEVELOPMENT STRATEGIES CORP.

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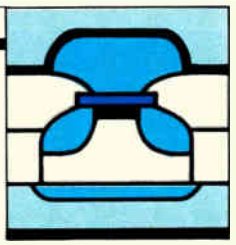


MOTOROLA'S BOMBSHELL— A RISC CHIP THIS SPRING

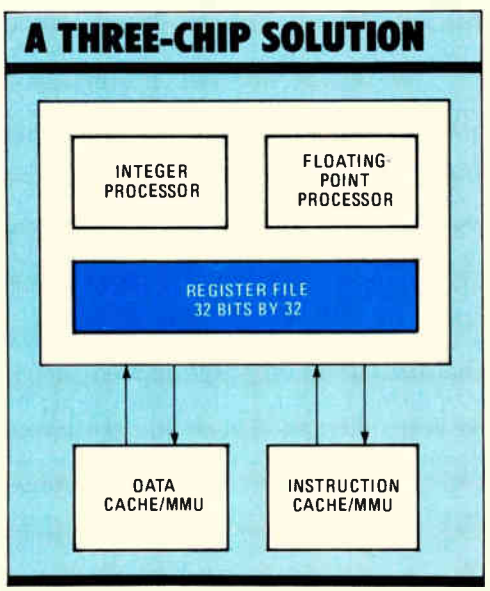
The chip maker saw silicon last year, and now it's almost ready to release a three-chip set, optimized for Unix, that will start out at 17 mips and could make systems that hit 50 mips

by Stan Runyon

Motorola Semiconductor Inc. is about to spring one big surprise on the electronics industry. While it's no secret that the U. S. chip leader has been working for a couple of years on a reduced-instruction-set-computer chip, only a few of its customers know that the chip maker saw silicon last year and expects to unwrap its product—a three-chip set—sometime during the second quarter of 1988.

Perhaps more surprising than the lightning-like speed of Motorola's moves is the comprehensive nature of the results. Not only will Motorola unveil a three-chip RISC set based on the Harvard architecture, but it will also offer a complete systems solution, including crucial development software. "We're going to provide everything from soup to nuts this year for the customer," says Jack W. Browne, Jr., marketing director of the company's High End MPU Division in Austin, Texas. Ready to go, for example, is a software simulator and a system to run Unix.

"People will be surprised at how complete our product offering is and how fast we're moving," Browne says. And here's an even bigger bombshell: Motorola already has two dozen customers committed to its new 32-bit RISC family; another 200 potential customers are evaluating it. The set—composed of a central processing unit chip and two cache/memory-management chips, one each for the instruction and data paths—will burst out of the gate fortified with architectural horsepower meant to leave the competition eating dust (see figure). "Working silicon is here, and we have measured its speed at 34,000 Dhrystones," Browne says. "We are projecting a rough rate of 17 working VAX mips to start, but we will show our customers how they can hit 50 mips this year." Sun Microsystems RISC chip—the scalable processor architecture, or Sparc—carries a 7- to 10-million-instructions-per-second rating [*Electronics*, Sept. 3, 1987, p. 72].



Motorola's 17-mips RISC chip set hinges on the classic Harvard architecture.

There appears to be plenty of performance headroom in the Motorola RISC—which will not be dubbed the 78000, its rumored designation. Carved out of 1.5-μm double-metal double-polysilicon CMOS, the set is scalable. It can go down to 0.8 μm, independently of the architecture, which has been optimized to run the Unix operating system, Browne says.

Despite all the heat and noise generated in the past year about RISC chips, "Motorola is not playing catchup," Browne maintains. Some observers have wondered just how the chip giant would enter the RISC market in a way that wouldn't hurt its lead in the 32-bit microprocessor market. But Browne sees no competition between Motorola's wildly successful complex-instruction-set 68000 family and its RISC chips, which are source-code—but not binary—compatible. "The issue is time to market, both for us and our customer. RISC's simplicity lets us quickly satisfy the speed craving and lets our customers streak into their markets with raw performance. The 68000, on the other hand, is in more of a price-sensitive market.

"There'll be no cannibalization of the 68000 market," Browne says. "We'll take the RISC business out of other people's hides." He is counting on Motorola's resources, reputation, and huge customer base. And he is quick to mention the more than $20 million that Motorola will spend this year alone in RISC development, not counting process

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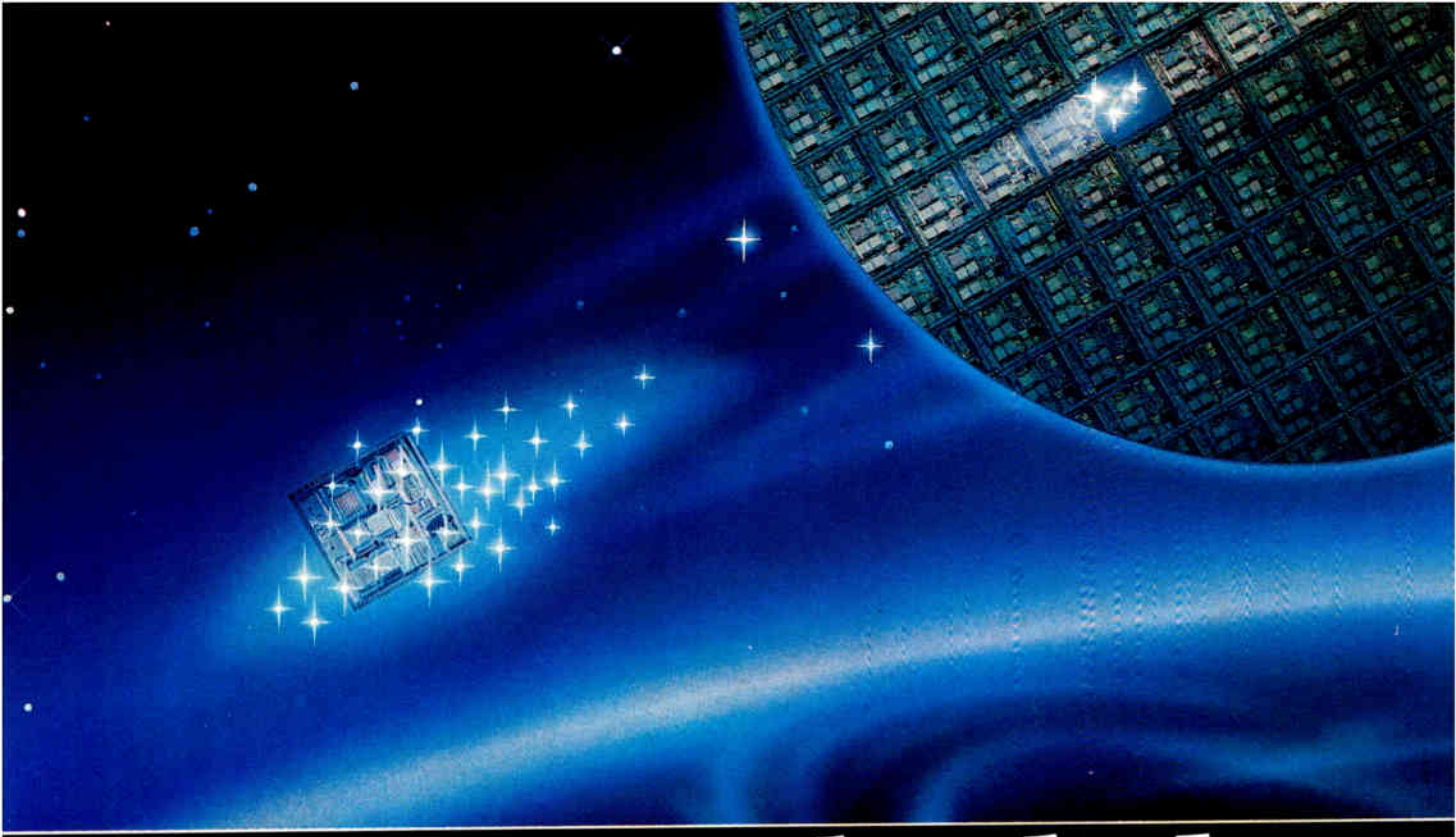

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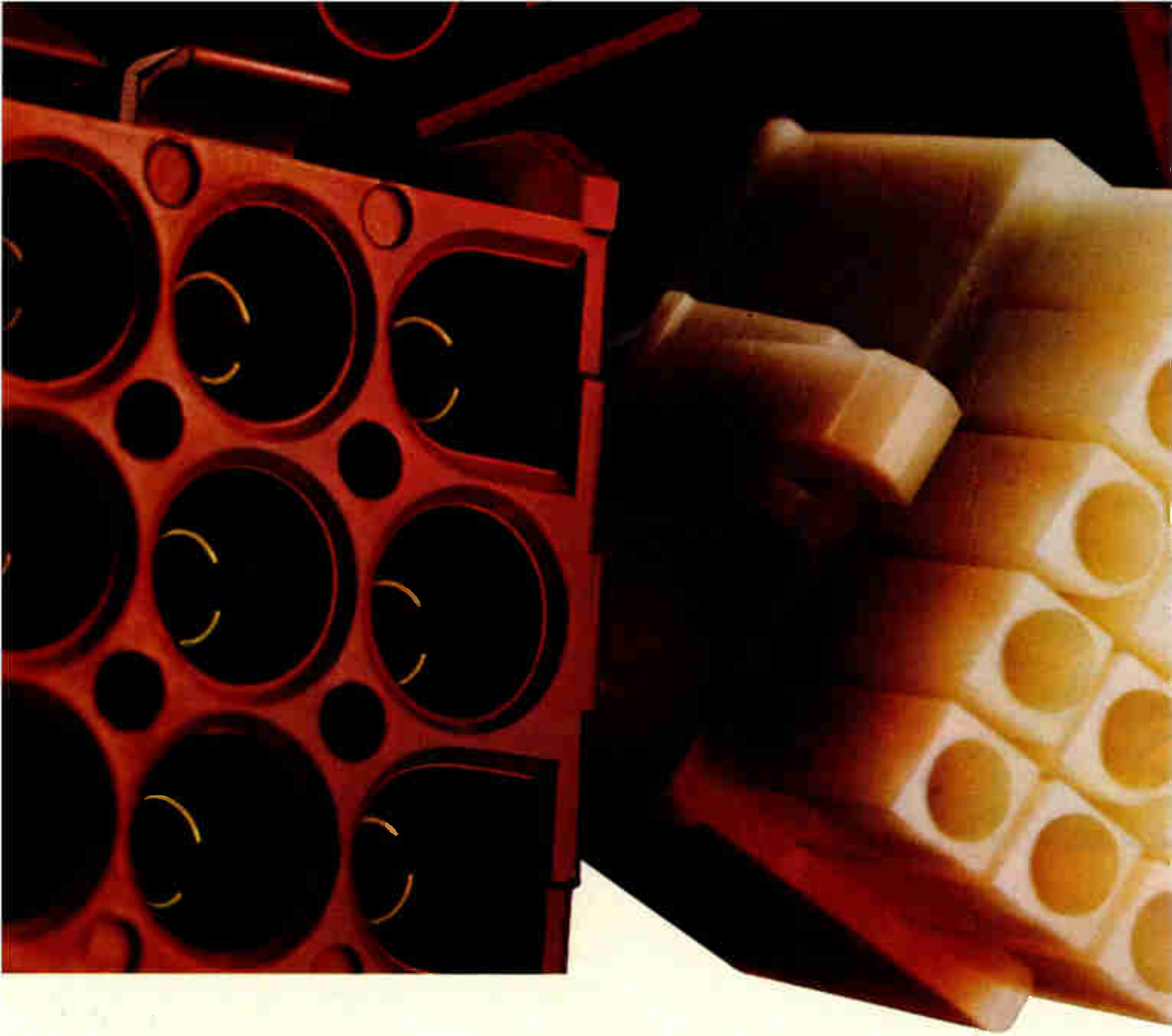

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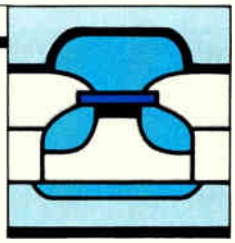
A NEW MEMORY TECHNOLOGY IS ABOUT TO HIT THE MARKET



Two startups are about to offer a new type of RAM, based on the ferroelectric effect, that will challenge nonvolatile memories by delivering speed and density as well as nonvolatility

A new kind of memory technology, exploiting the well-known but little-used ferroelectric effect, may be the key to the ideal memory device: nonvolatile, fast, dense, and radiation-hard. The technology is about to emerge in the form of products turned out by two startups: Ramtron Corp. of Colorado Springs, Colo., and Krysalis Corp. of Albuquerque, N. M. [*Electronics*, Feb. 4, 1988, p. 32]. The following two Technology to Watch articles delve into the Ramtron and Krysalis approaches to ferroelectric random-access memories.

Nonvolatility is inherent in ferroelectric memories, and if these new RAMs deliver the promised read/write speeds and long life, they could largely supplant erasable programmable read-only memories and electrically erasable PROMs, says Howard Z. Bogert, vice president of Dataquest, the San Jose, Calif., market research firm. Furthermore, he says, they could be a threat to dynamic RAMs. They are relatively simple—a 4-Mbit ferroelectric RAM could be built without trench capacitors, for example—and it is possible that further development could bring their cost and their read/write times down into DRAM territory.

All this is being claimed for devices built around the ferroelectric effect. Although the ferroelectric effect was discovered in 1921, it was poorly understood until the 1960s. Iron has nothing to do with the effect. The prefix "ferro" originated with early attempts to describe the phenomenon, which assumed that the ferromagnetic properties of some iron-bearing compounds were involved.

The ferroelectric effect is the tendency for certain crystalline materials to spontaneously polarize under the influence of an externally applied field and remain polarized after the field is removed. Reversal of the field causes spontaneous polarization in the opposite direction. So ferroelectric materials can be modeled as bistable capacitors with two distinct polarization voltage thresholds.

No external electric field or current is required for the ferroelectric material to remain polarized in either state, so a truly nonvolatile ferroelectric "digital memory capacitor" can be built for storing 1s and 0s. Data stored in a ferroelectric memory element can be read by sensing the interaction of an applied field with the element's polarization.

In practice, ferroelectric materials do not polarize instantaneously, and polarization thresholds are not perfectly defined. Most early ferroelectric research concentrated on finding materials with better characteristics. Those efforts were unsuccessful, but now Ramtron and Krysalis, working separately, say they have made the breakthroughs in materials, processing, and circuit design that will turn ferroelectrics into commercial reality.

FERROELECTRIC CAPACITORS ARE RAMTRON'S BRIGHT IDEA

They act as backups for SRAM cells, storing logic states when the power is interrupted

It took an all-out research-and-development effort in circuit design and semiconductor processing, as well as in materials, to make the breakthroughs required to manufacture practical ferroelectric devices, say researchers at Ramtron Corp. The Colorado Springs, Colo., startup has devised a static random-access memory that achieves nonvolatility by using backup ferroelectric capacitors to store logic states during power interruptions.

The result is what Ramtron calls a ferroelectronic RAM, or FRAM. Its first chip—a 256-bit nonvolatile static RAM—will be introduced at the Feb. 16-19 International Solid State Circuits Conference in San Francisco. It is the forerunner of a family of larger FRAM products, including 16- and 64-Kbit memories due out later this year and 256-Kbit devices slated for 1989.

"The FRAM is the world's first true nonvolatile read/write memory," says Richard Horton, Ramtron's director of business development. "The breakthrough technology is expected to have a

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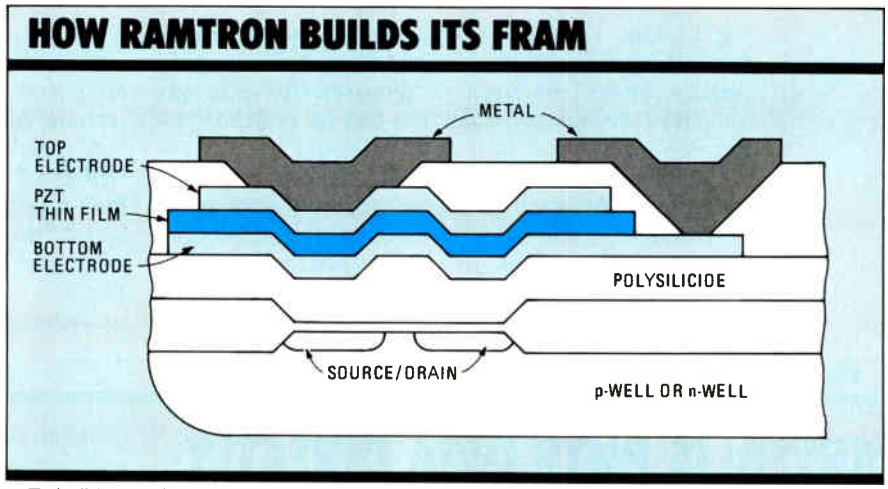
ed, the transmission gates are turned on, connecting the ferroelectric capacitors to the cell inputs and polarizing them to the RAM cell state prior to power loss. Sufficient polarization for nonvolatile recovery occurs within 10 to 20 ns, well before the RAM loses its state or the power supply collapses. Once charged, the capacitors can retain their state almost indefinitely.

Recovery from power loss and return to active RAM mode are also direct. As power is applied, the capacitors strongly bias the inputs of the RAM cell to reflect the stored condition. Once fully powered, the transmission gates are opened, removing the ferroelectric capacitors from the circuit and leaving the RAM in the same data condition that it was in prior to power loss.



3. To build capacitors—the nonvolatile storage elements—on top of a silicon-gate MOS FET, Ramtron adds two electrodes with a PZT thin film in between.

The design eliminates the traditional problem of fatigue in ferroelectric memory, which until now has limited its use to about 10^{10} cycles. Most previous experimental designs relied on ferroelectronic polarization for every write cycle, making them impractical for the majority of main memory applications. In the FM801 and the first generation of commercial devices, an endurance cycle of 10^{10} is more than adequate, since ferroelectric polarization occurs only during power sequencing. This means that the FM801 has a life expectancy exceeding 27,000 years, even if a power loss occurs 10 times per day. And early test results suggest that lifetimes of 10^{15} cycles are possible. Longer endurance will allow ferroelectric storage to be built into the active memory circuit, replacing the dynamic capacitor storage used in DRAMs.

Virtually all of the FRAM's external characteristics are identical to those of standard SRAMs. Read and write cycles are symmetrical and as fast as a SRAM's: the FM801 has an access time of 70 ns, while the upcoming commercial parts will boast 20- to 40-ns speeds.

Like the FM801, these devices will also be based on the six-transistor SRAM topology, and will include 2-K-by-8-bit and and 8-K-by-8-bit configurations in standard Jedec packaging. They will be directly pin-compatible with current 5-V SRAMs and EEPROMs. For the next generation of 256-Kbit models, Ramtron is developing an optimized, merged technology eliminating redundant metallurgical steps. When the merged process is coupled with a one-transistor cell design, (see fig. 2b), FRAM manufacturing costs will approach those of DRAMs.

As with the circuit design, the FRAM fabrication process is simple and straightforward. The base circuitry of the FM801 is built using a conventional 3-μm silicon-gate CMOS ASIC process, with a single level of metal interconnection (see fig. 3). No process adjustments to the underlayers are reqired to add the ferrolectric process steps. Three process steps must be added to the base circuitry: two layers of metal for electrodes and a thin film of a ceramic lead zirconate titanate. The metal-PZT-metal sandwich produces what might be called a digital memory capacitor, which is the nonvolatile storage element. This is a new component for circuit design—Horton says it as fundamental as the field-effect transistor. Connection to the base circuitry is made using conventional metalization and vias to the underlayers.

The ferroelectronic layers can be added directly over active devices. The result is a true three-dimensional circuit, built vertically over standard semiconductor devices. Ramtron's ferroelectronic process is complementary to current semiconductor processes, including bipolar and CMOS silicon, as well as to gallium arsenide, silicon on insulator, and others. All of the physical and electrical features of the underlying circuitry are preserved, and no additional area is required. Further, logic compatibility can be programmed over a wide range by varying the PZT film thickness and metallurgy, making ferroelectronics largely independent of the substrate and underlying process.

The PZT material itself has highly desirable physical and electrical properties. Among them are high resistance, since its tight crystal lattice makes it an insulator; thermal and chemical stability, because it is almost unreactive chemically, and has a Curie—or phase-change temperature—exceeding 350°C; and because it has the hardness that is typical of ceramics. Ramtron's PZT remains nonvolatile from –180° to above +350°C, well beyond the operating temperature range of existing silicon circuits. And breakdown voltage of the PZT film is high; the film used for CMOS-logic compatibility easily withstands 40 V. In addition, it is highly resistant to radiation.

Another advantage of the PZT material is very high dielectric constant, which at 1,200 is roughly 300 times that of the dielectric used in exist-

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electric capacitors, which can be changed by an applied electric field to store digital data states.

Krysalis will not reveal details of its process or the ferroelectric material it uses. The firm will say only that the material is a perovskite crystallization structure that is a derivative of lead zirconate titanate, which is deposited using a method compatible with conventional semiconductor-processing techniques. The ferroelectric thin film will add about 5% to 10% to the cost per wafer of a standard 12-mask CMOS process, the company says. Currently, it takes three masks to form the ferroelectric cells, but later designs could need only one additional mask step to integrate the ferroelectric with the silicon, according to Krysalis.

The company's chips differ in some respects from Ramtron's initial parts. Whereas the Ramtron devices will rely on conventional six-transistor static-RAM silicon cells that are "shadowed" by nonvolatile ferroelectric memory, the Krysalis UniRAM line will use the ferroelectric as the primary storage element. "Our technology is a direct RAM, where every [write and access] cycle talks to the ferroelectric cell," says William Miller, vice president for process development. "Every time you write, you write to the ferroelectric memory, and therefore, it's always nonvolatile. You never have to worry about doing a store before a power down, or having to do a power-fail detect."

The approach also pays dividends in cost and density, Miller says. Instead of a six-transistor SRAM-type silicon cell plus the ferroelectric elements, the Krysalis cell contains only a single transistor and a single ferroelectric capacitor. The 16-Kbit products will employ a double-ended scheme requiring two cells, or four devices, per bit. But subsequent 64- and 256-Kbit UniRAM parts will use a different approach requiring only one cell per bit, further improving density, Miller says. Samples should be available in early 1989.

In the Krysalis 512-bit demonstration chip, the double-ended cell scheme creates a self-referencing signal differential across the sense amp (see fig. 2). The memory bit consists of a word line controlling two pass transistors, a bit line, a $\overline{\text{bit}}$ line to collect charge from the capacitors, and a common drive line to actively drive the capacitors. A sense amp resides between the bit line and the $\overline{\text{bit}}$ line.

For a write, the sense amp is set to the desired state, and the bit and $\overline{\text{bit}}$ lines are driven to the opposite voltage values of V_0 and ground. The drive line is pulsed in such a way that the high drive line against the grounded bit line writes the 0 state into its capacitor. When the drive line drops to ground after the pulse, the other capacitor has a 1 written in it by its high bit line voltage.

In the read operation, a voltage step is applied to the drive line with the bit lines floating and the sense amp off. Since the capacitors are in opposite states, the bit line and $\overline{\text{bit}}$ line will collect different amounts of charge and produce a voltage differential of a polarity determined by the stored data. The sense amp then turns on to capture the bit. With the sense amp on, the bit lines are driven to the opposite rails and the destructively read bit is automatically restored. The restore is invisible to the user and occurs in parallel with the output gating of the read data to the input/output ports.

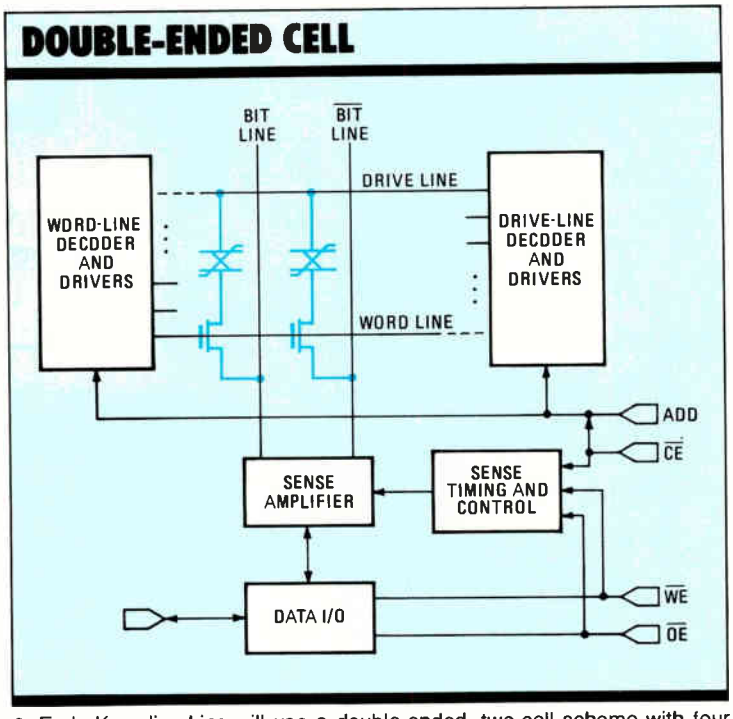
The memory array in the 512-bit part is arranged as 64 rows of 8 bits apiece with no column decode. One row consists of 16 capacitors sharing a common word line and drive line and arranged as eight double-ended memory bits. The part also includes on-board test circuitry.

Its capacitors measure approximately 5 μm by 9 μm, are less than 1 μm thick, and have nominal capacitance of 1 picofarad apiece. The drive-line and word-line drivers are located on either side of the memory array. Regenerative feedback amplifiers similar to those in DRAMs constitute the sense amps. The device has standard three-state I/O functions.

Buffered inputs control the word line, drive line, sense amp, and equalization functions. In combination with the I/O controls, the device requires seven timing inputs, a setup designed to allow experimentation with timing algorithms. However, the Krysalis 16-Kbit parts will be offered with standard SRAM three-line control.

Likewise, the 512-bit part requires both a 5-V power supply and a second 7.5-to-10-V supply. But the commercial 16-Kbit parts will operate on a single 5-V supply. *–Wesley R. Iversen*

For more information, circle 481 on the reader service card.



2. Early Krysalis chips will use a double-ended, two-cell scheme with four devices per bit; later versions will have one transistor and capacitor per cell.

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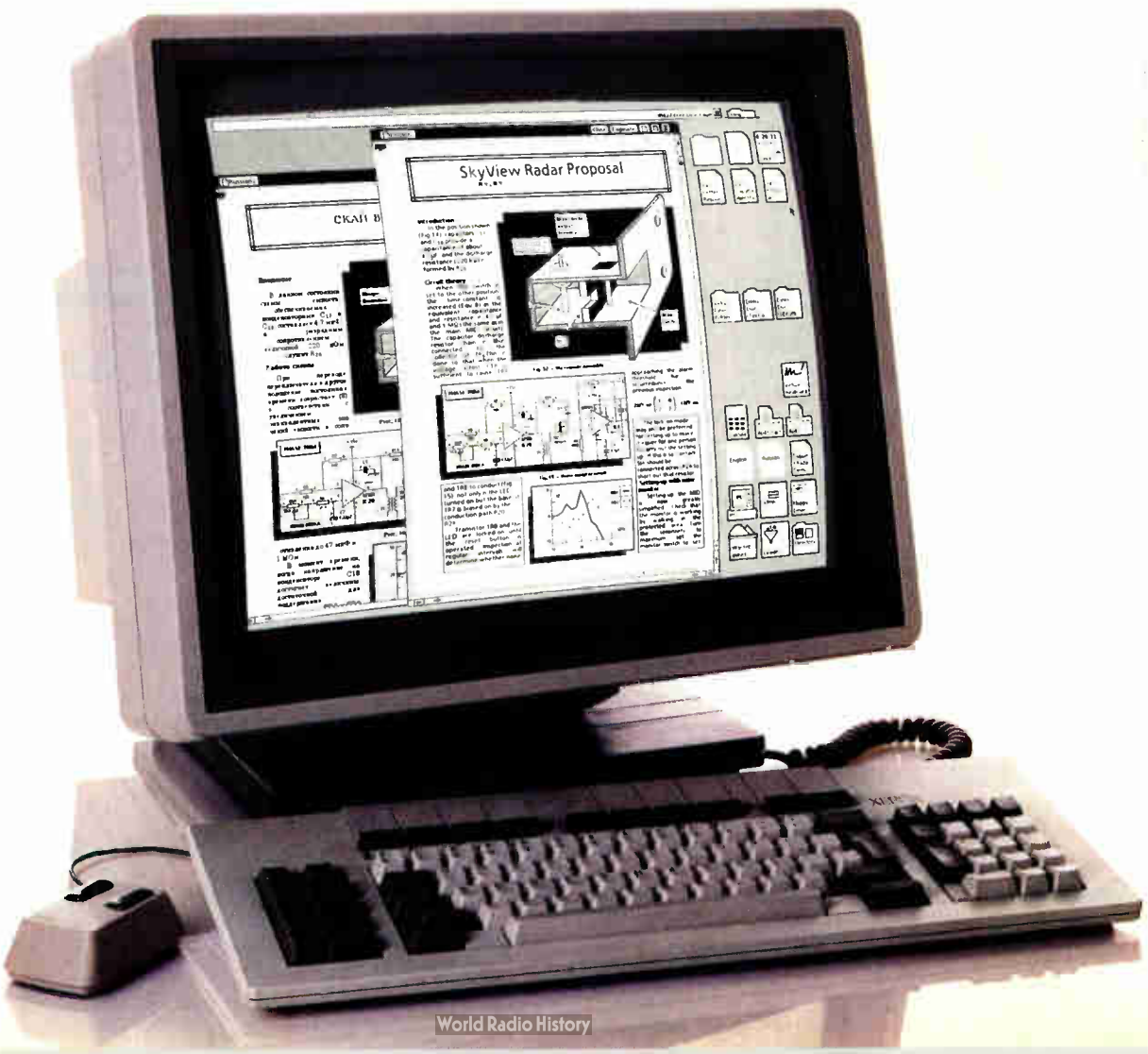

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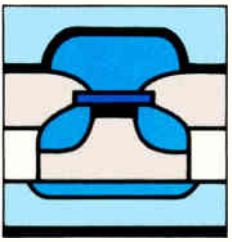


ALTERA'S SPEEDY WAY TO TAILOR ADD-ONS TO IBM'S PS/2

Its newest EPLD gives board makers a working interface to the PS/2's bus, cutting time to market and saving board space; when used with a companion DMA chip, it replaces 18 components

by J. Robert Lineback

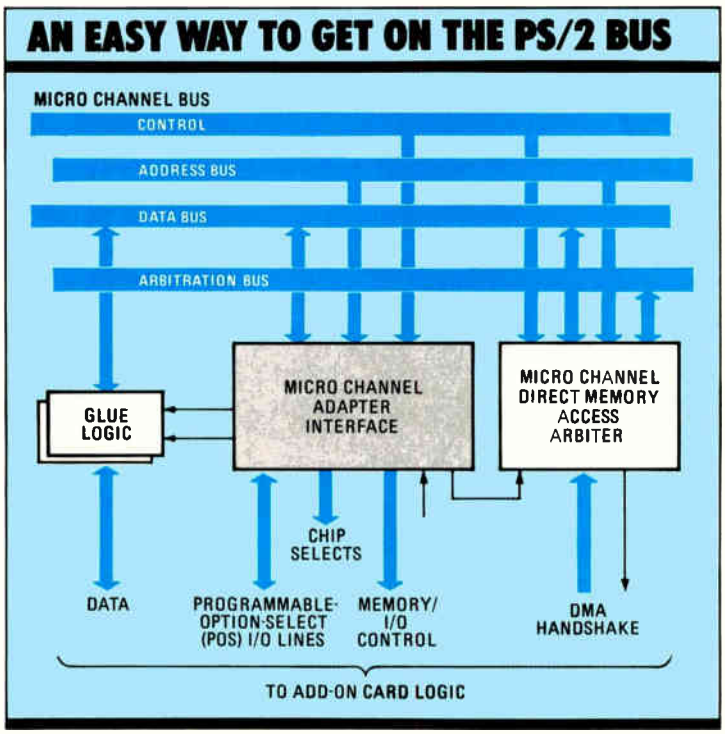
Add-on board suppliers will soon get an all-in-one programmable interface chip that will help them quickly enter the potentially huge market for plug-in peripheral cards serving IBM Corp.'s Personal System/2 and its widely expected clones. Altera Corp. is launching the industry's first erasable programmable logic device aimed at providing a complete interface to the IBM Micro Channel bus. Not only will the new CMOS EPLD save time in turning out the add-on boards, but it will save board space as well. Accompanying development software will cut the time to market even more, and vendors will be able to put their add-on PS/2 interface functions into four reserved programmable spaces on the EPLD.

The newest function-specific chip from the Santa Clara, Calif., company gives board vendors a working interface (see fig. 1) to the Micro Channel for any of a range of peripheral cards, including tape and disk controllers, communication links, special graphics capabilities, data acquisition, and multifunction plug-in cards. Compared with existing nonprogrammable Micro Channel chip sets and emerging mask-programmable semicustom interfaces, the EPB2001 should dramatically reduce the board space required to meet IBM's complex new logic and timing specifications.

Initial shipments of the software, the 2001 EPLD interface chip, and a companion 28-pin direct-memory-access arbiter are slated for the second quarter. The 2002 arbiter chip is Altera's first nonconfigurable integrated circuit; the firm opted to leave the DMA's functions off the 2001 because about half of the anticipated applications will not require such features. Volume production of both chips will start in the second half of 1988. In 10,000-piece quantities, the 2001 interface device will cost less than $12 each, says David A. Laws, vice president of marketing at Altera, and the 2002 will go for $5.

The Altera package is after a big market. About 400,000 PS/2s equipped with Micro Channel were shipped last year and another 800,000 should be sold by the end of 1988, Laws estimates. On average, each Micro Channel-based PS/2 will get three plug-in cards within 18 months, Altera estimates.

And because of the EPLD, the company thinks, many of these PS/2 users will have additional, cost-effective options available to them. "With our user-configurable interface, add-on board manufacturers can quickly prepare prototypes or launch small-to-medium-volume products without taking on the expense of custom circuits," says Laws, who notes that the PS/2 plug-in boards are about 40% smaller than the cards for IBM's Personal Computer AT and compatible PC models. "The cost of custom circuits [to reduce the Micro Channel interface logic or the peripheral function's own logic] could keep some startups from getting start-



1. Altera's new EPLD and some glue logic are all that are required to get on the Micro Channel bus. The DMA chip is optional.

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brary. This contrasts sharply with other systems, which restrict block placement. Some will only place large blocks in the corners of the layout. Others will not allow the use of oddly configured blocks, such as L-shapes, U-shapes, and C-shapes, but will accept only rectangular blocks. In addition, some other systems place blocks only roughly, so that the designer must correct the placement before a router connects the blocks.

Chip Crafter not only provides complete freedom in placing large blocks of cells, but also provides greater latitude in what goes into the blocks

Besides more flexibility in placing blocks, ChipCrafter provides greater latitude in what goes into the block. When a design calls for using standard and megacells in the same layout, ChipCrafter need not simply gather standard cells into one or more large blocks, as other systems do. It can leave the standard cells as a single block or divide them into multiple blocks as needed to create the most efficient floorplan. The system therefore can sprinkle them in whatever open spaces exist between blocks, on the basis of connectivity and the most efficient placement.

ChipCrafter lays out in two passes. During the first, it determines optimum placement for blocks and standard cells, given the interconnection list and the size and shape of the blocks. It then routes the blocks and cells. The system also calculates the number of outputs any one gate will drive (fanout) and the load the fanout places on the gate's output driver stage. To get the best performance, ARAR+ matches the outputs of individual blocks to the length of line at each output and the load at the end of each line.

During its second pass, ChipCrafter takes information attained in the first pass and makes the transistors inside all of the nonrectangular blocks and standard cells larger or smaller, to match the loading and fanout conditions derived in the first pass (see photos, p. 101). Of course, when the size of the transistors inside a block is changed, the blocks change in size and shape, too. So the system performs a second place and route, readjusting the layout to accommodate the changes. "No other layout tool available can dynamically resize transistors inside a large block," Morrell says. *–Jonah McLeod*

For more information, circle 483 on the reader service card.

TECHNOLOGY TO WATCH **CAD/CAE**

CATCHING GLITCHES AND DELAYS IN DENSE ASIC DESIGNS

SMOS Systems uses expert-system technology to find and display bugs, cutting a week off design cycles

A new generation of design tools from SMOS Systems Inc. will make it much easier to get rid of harmful glitches and cut down timing delays in application-specific integrated circuits. Both glitches and timing delays have become far more serious problems as ASICs move toward 1.2-μm or finer geometries and clock rates grow faster. Glitches, or noise pulses, can upset complex logic designs and cause system failure. Timing delays can disrupt the chip's operation, and trying to avoid them on a dense chip makes component placement in a design a nightmare for designers.

The LADDS 5.00 series E—an upgrade of the San Jose, Calif., company's LADDS 5.00 series D set of design tools—automatically finds glitches and delays in signal paths that can prevent a gate from functioning. It also contains a place-and-route-tool that, operating automatically after a single pushbutton command, produces a layout that is completely routed with its timing corrected.

The software runs on IBM Corp. PCs and compatibles, Digital Equipment Corp. MicroVAXes, and Intergraph work stations. Available now, it is provided at no charge to a designer with an SMOS foundry service contract. The tools work with SMOS's CMOS processes only—the company is a high-volume foundry which typically contracts for a minimum order of 10,000 devices per month using gate arrays and standard cells.

To guard against glitches, the series E simulator uses expert system technology. It finds those glitches that might produce an error—all others are ignored—and presents them to the designer on a display. The designer then determines which errors need to be removed and which can be ignored.

With the glitches eliminated, the designer can evaluate the functioning of his logic design without having to debug it. After debugging, the designer performs another simulation, and the simulator shows the designer what his circuit does with noise pulses propagating through the design.

Working with densities of 2-μm or more in CMOS, the designer could usually catch all these glitches unaided. "The larger-geometry CMOS processes were very forgiving, so the number of glitches that had to be debugged during simulation was relatively small," says John Conover, director of engineering. "With the advent of 1.5-μm and smaller-geometry CMOS, the problem has become too complex to be done effectively without the simulator."

And the simulator needs expert-system technology to work effectively. When it's simulating a

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circuit implemented in fast process technologies, the simulator produces a file containing a huge number of detected glitches. "A glitch file can have several megabytes of data," Conover says. Without a smart simulator, the designer must wade through the file line by line, examining each glitch to determine its effect on circuit operation.

By contrast, the expert system in the SMOS simulator compares the debugged model of the circuit with the model containing the detected glitches. It then performs the line-by-line analysis and presents to the designer those glitches which are most likely to affect circuit operation. The expert-system software will err in favor of catching too many errors, rather than leaving a catastrophic error in the design. But the designer makes the determination of which glitches are significant. "This software aid will cut from one to two weeks out of a design cycle," says Conover.

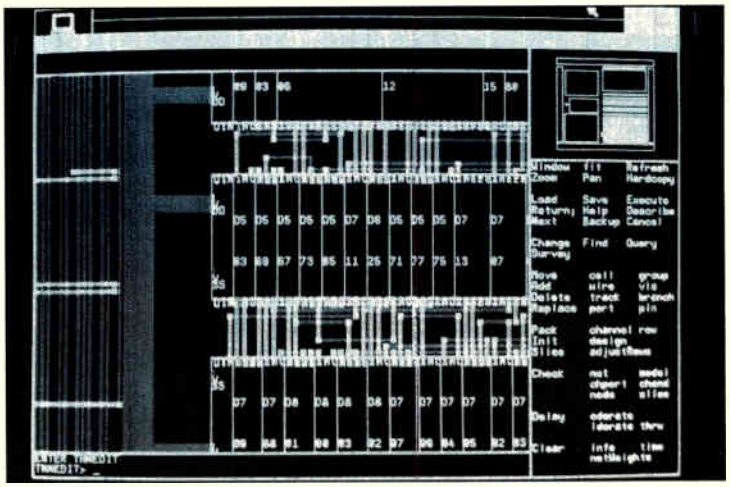
There are two ways for the designer to work with the simulator. One is interactively: the designer gets a display on the design system's cathode-ray tube. On encountering a glitch, the system highlights the error on the display (see photo) and asks the designer whether to ignore or to propagate it. In interactive mode, to aid in evaluating the glitches it has culled, the simulator allows the designer to examine a single glitch at a time (or any other number desired) and propagate it backward or forward through the system. The process repeats for all the glitches culled by the expert system. If the glitch is propagated, each error produced by the propagated glitch is highlighted for the designer to evaluate. He can evaluate each glitch individually without confusing one with another.

The simulator also operates in batch mode. "Most designers prefer to run the entire simulation at once, with no interaction," Conover explains. "At the end of the run, the simulator creates a file containing the significant glitches. The designer then refers back to his schematic to evaluate the impact of each of these glitches."

With the glitches detected and, where necessary, eliminated, the designer can start to work cutting down timing delays, by evaluating set-up-and-hold violations. In 2-μm process technologies, the difference in arrival time for two pulses at the input of a gate due to timing delays in the lines leading up to the gate was insignificant. Now, with faster 1.2-μm CMOS, the difference in delays can produce meaningful errors. The gate delay—amount of time required for a pulse to pass through a gate—is 1.29 ns for 2-μm CMOS; the gate delay for 1.2-μm CMOS is 0.53 ns.

If he has to do the job by hand, the designer must trace a signal through the circuit and add and subtract delays in the data path of one or both signals to ensure the D input reaches the flip-flop at the right time relative to the clock input. The process is repeated for all the flip-flops which have a set-up-and-hold violation.

"With the expert system capability added to the tool, this function occurs automatically," Conover says. "The tool alerts the designer if the time relationship between the D-input and clock of a flip-flop is inadequate. It specifies the faulty flip-flop and when the set-up-and-hold violation occurs." The designer corrects all the set and hold violations as well as all the glitches, performs a logic simulation, and then passes the file to the place-and-route tool for automatic layout.



PLACEMENT. SMOS's system places cells relative to one another to conform to design timing specs and to eliminate glitches.

In the faster CMOS process technology, wire length becomes a contributing factor to violations of set-and-hold-times as well as other timing anomalies. A typical place-and-route tool in an ASIC design tool kit lays out a debugged schematic it receives from the front-end design system. Then it sends the design simulator a netlist containing the circuit timing resulting from the layout. If the timing simulation shows that the layout altered the circuit, the designer must adjust the layout to eliminate the problem. The LADDS place-and-route tool differs from this approach in that it is a timing-driven layout system. Before any layout is undertaken, it looks at the simulation from the front end system to determine the timing constraints. It then makes a layout that meets these constraints.

In creating a layout, the system assigns 2 mm of aluminum for each interconnection on the chip. "On a chip with 30,000 gates, the 2-mm figure is a good, conservative number," Conover says. "There are not likely to be many wires that long in a chip layout. If the circuit works with this conservative wire length, it will work in any condition in the circuit." The layout system knows, in effect, that in some instances it must create a wire length longer than 2 mm. If it must make placements which exceed the simulated 2-mm length, the system determines if the longer wire violates the timing specification of the device. If it does, then the tool alters the placement to shorten this wirelength to an acceptable length. *—Jonah McLeod*

For more information, circle 484 on the reader service card.

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deliver a paper on achieving accurate placement of fine-pitch surface-mount devices through measurement and feedback at the time of placement. The paper describes a new system in which four video cameras measure the placement error at each of the four corners of a fine-pitch package. The four views are displayed simultaneously on a monitor to the operator, who can then adjust the position of the machine's placement table to reduce the alignment error. Drislane notes that SR Technologies is currently developing a next-generation system using machine vision to close the adjustment loop—in other words, it will correct alignment errors automatically. This system is applicable to gull-wing and flat-pack package types, as well as leadless ceramic carriers.

A real-world application of a modified SR Technologies semi-automatic system is dicussed in the session's closing paper. Donald R. Mullen of the Evans & Sutherland Computer Division, Mountain View, Calif., tells how the system is used for surface-mount placement and soldering of a square gull-wing package measuring 2 ½ in. on a side. The package has 340 leads on 25-mil centers.

Thus, surface-mount packages with very high lead counts are clearly headed for practical commercial use. So too is a whole new family of oddly shaped molded thermoplastic pc boards. A raft of real-world applications of this technology are described in a standout Nepcon session on the commercial applications of production facilities for 3-d molded pc boards.

A paper from Xetec Corp., Salinas, Kan., for example, describes the use of 3-d molded board technology (furnished by DuPont) in solid-state ballasts for fluorescent lighting. Another paper, from Smith-Corona Corp., Cortland, N. Y., discusses the use of technology from Pathtek Inc., Rochester, N. Y., for constructing molded boards for a light-emitting-diode assembly used in an electronic typewriter. The approach is said to result in substantial savings in parts, labor, and tooling.

Two papers from the ICI Electronics Group an operating company of ICI America, Wilmington, Del., cover 3-d molded boards for brushless motors and a connector for a telecommunications application. In one of the papers, John Williams and John Haffey of ICI discuss the review process of the requirements for two brushless-motor circuit boards for two different customers. One of the resulting molded-plastic boards is a circular one for a disk-drive motor; the second is a shaped board that replaces a more expensive flexible circuit.

A second paper by Sean McKinley of ICI and Gary Nault of ADC Telecommunications Inc., Minneapolis, talks about the requirements and the fabrication of a four-wire patch plug for testing the main boards of telephone exchanges. ADC formerly used a version of this plug made of FR-4 glass-epoxy material. This unit had poor reliability, a short life, and problems with frequent breakage. The 3-d board, thanks to the ruggedness of ICI's polyethersulfone (Victrex) plastic, increased reliability and board life by at least a factor of three, according to the paper's authors. Furthermore, it cut costs by eliminating the need for a separate connector—a connector is an integral part of the molded pc-board assembly.

As board-manufacturing and packaging technologies advance, new problems must be solved by test and inspection engineers. One Nepcon session on inspection and another on test show how some of these challenges are being tackled.

Nepcon will also hear about a raft of new test and inspection solutions

The inspection session features papers by Nicolet Test Instrument Division, Madison, Wisc., and IRT Corp., San Diego, on X-ray techniques for inspecting assembled pc boards. "Electrical testing often gives only half the story for boards loaded with certain types of packages," says the chairman of the inspection session, Edward Soron of IRT. Pin-grid-array packages and leadless chip carriers have many solder joints that are can't be inspected, for example, and plastic leaded chip carriers with J-leads bent under the body of the carrier are extremely difficult to inspect.

The only way to find out whether the barrel of a hollow PGA socket pin on a pc board is full of solder is by using transmissive X-ray techniques, says Soron. The same radiography technique is needed to check the solder fillets of leadless ceramic chip carriers.

Trace Instruments, a division of Methode Electronics Inc., Canoga Park, Calif., covers a problem testing area peculiar to today's high density, fine-line pc boards—board damage caused by testing.

The effects of various stimulus voltage and current levels on fine-line bare boards, hybrids, and substrates are examined in a paper given by George Hroundas of Trace Instruments. Strict control of these parameters is vital if testing is not to degrade or destroy board interconnections. The way test stimulus voltage affects both conductor integrity and isolation resistance is explored along with the cost consequences of less-than-optimum testing strategies and parameters. □

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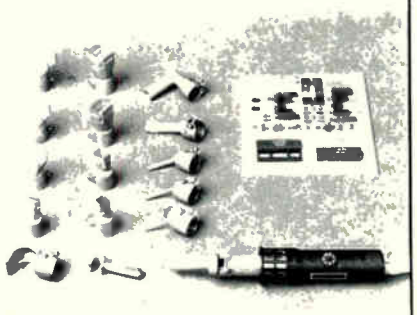

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American dance is more popular than ever, and one of the reasons is The New York Public Library's Dance Collection.

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MILITARY/AEROSPACE NEWSLETTER

SURPRISE! GE BEATS OUT IBM TO DEVELOP SUBMARINE COMBAT SYSTEM

In a surprising development, General Electric Co. beat out IBM Corp. for a much-coveted contract to develop the combat system for the Sea Wolf, the Navy's next-generation attack-class submarine. The decision was a major disappointment for IBM, which is the prime contractor for the AN/BSY-1 combat system on the current generation of attack-class subs [*Electronics*, Nov. 26, 1987, p. 148]. The BSY-2 contract is particularly valuable because of the long design cycle involved—the first Sea Wolf won't be launched before the year 2000. Moreover, BSY-2 had been a major focus of IBM's work in its Very High Speed Integrated Circuit program. Development of a set of four chips designed for an advanced sonar system was a key part of the company's effort in VHSIC's second phase [see story, pg. 37]. The award to GE of an initial $13.6 million contract to guide BSY-2 from the design definition phase into full-scale engineering and development won't leave IBM out in the cold, however. An IBM spokesman says the company expects to join GE and its teammates, Computer Sciences Corp., Martin Marietta Corp., and Singer Co., in a follow-up role later this year. □

THE ARMY WANTS TO MOVE TECHNOLOGY FASTER INTO MILITARY SYSTEMS . . .

The Army Science Board is worried that new technologies aren't finding their way into Army systems fast enough, so it is sponsoring a six-month study on how to speed up the process. The board has charged an 18-member panel with producing a set of recommendations by July and a final report for public release by October. The group, which will be chaired by Paul W. Kruse Jr., chief research fellow at Honeywell Inc., Bloomington, Minn., will meet for the first time late this month to try to focus its attention on a few vital technologies. It is expected to zero in on the Defense Department's Very High Speed Integrated Circuit program. Developed to advance military electronics, VHSIC chips have yet to find wide application in military systems. □

. . . AND CUT THE SPIRALING COSTS OF TESTING

Testing procedures for military components and systems have been criticized for years for everything from being too easy to too expensive. The problems have sparked the Army Science Board to order a study on testing strategy. A science board panel will report this summer on "how we go about testing components and systems," says Col. Richard E. Entlich, the board's executive secretary. The panel will analyze testing procedures and make recommendations on more cost-effective testing. "Sometimes we actually overtest," he says, adding that the Army can't afford that luxury. □

VARIAN IMPROVING TEST GEAR TO BOOST YIELDS ON GaAs DIODES

Varian Associates Inc., Palo Alto, Calif., is developing manufacturing techniques for Gunn and varactor diodes that it says will boost yield by a factor of three. The diode chips are key components in the Army's Sense and Destroy Armor munitions program, and Varian is supplying them to both Honeywell Inc. and Aerojet Electro Systems Co. The challenge is that the parts are so small—8 to 10 mils^2—and the specifications so tight that imprecise positioning during such manufacturing steps as wire-bonding and radio-frequency testing can cause perfectly good parts to fail, says Michael Kopec, sales manager for Varian's III-V Device Center. In addition, GaAs chips are brittle and break easily during testing. The company is taking basic equipment and "optimizing the positioning systems so they don't smash the chips into oblivion," Kopec says. He expects the new equipment will help Varian push overall yield of qualified wafers into the 50% to 70% range. □

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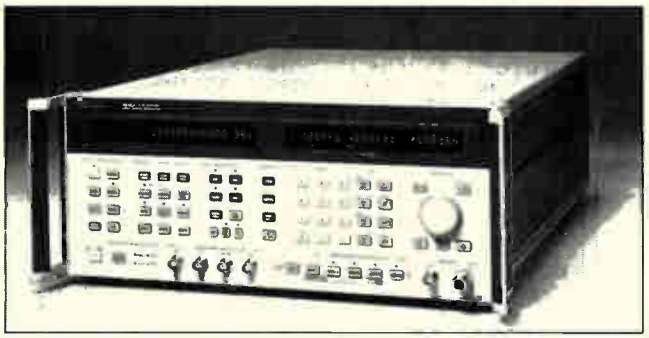
NEW PRODUCTS

HP HALVES THE COST OF INSTRUMENTS THAT TEST FREQUENCY-HOPPING RADIOS

THE 8645A IS A ONE-BOX ANSWER TO WHAT HAS BEEN A CUSTOMIZED SETUP

Makers of frequency-hopping radios for military and other security-oriented applications now have a single instrument that simultaneously evaluates both the radio's hopping and its transmission performance—and does so at less than half the cost of a customized solution.

Since frequency-hopping-radio technology is a relatively recent development, the appearance of Hewlett-Packard Co.'s HP8645A saves users from custom-designing a test setup that would—for starters—include a frequency-hopping local oscillator costing between $15,000 and $80,000, plus an FM modulator, which can run between $15,000 and $30,000. By contrast, the HP8645A costs $32,000.



PERFORMER. HP's 8645A operates from 250 kHz to 2.06 GHz and can change frequency every 15 μs with an accuracy of 1 Hz per MHz.

RF SIMULATOR. The 8645A can also simulate a complex rf environment for users who want to test receivers for susceptibility to interference. The instrument is equipped to test the fastest receivers. It operates over a frequency range of 250 kHz to 2.06 GHz and can change frequency every 15 μs with an accuracy of 1 Hz per MHz.

Extending the range down to 8 MHz increases switching speed to 85 μs. Below 8 MHz, the switching speed is 500 μs. Users can enter up to 2,400 unique frequencies and sequence through 4,000 frequency settings.

Frequency-hopping radios are becoming increasingly important aspects of communications technology across all branches of the military. Analysts peg the market for secure communications at $2.6 billion in 1986 and see it soaring to $7.5 billion by 1992, HP says.

Part of the reason for this anticipated boom is that advanced frequency-hopping radios have been developed in programs such as the U.S. Sincgars (for single-channel, group-to-air radio system) program, which created a backpack-portable radio for the infantry. It is expected to account for the production of several hundred thousand units. In addition, the Department of Defense's Jtids (for joint tactical information system) program has produced a larger transportable unit for mobile command posts and ships.

HP's 8645A offers a wide, versatile set of test functions while producing high-fidelity signals at precise frequencies. When measuring in-channel distortion, sensitivity, and hum and noise, for example, it delivers simultaneous fm, am, and pulse modulation with less than 2 Hz of residual fm. Signals with less noise and lower residual fm offer less interference in the measurement, reducing measurement uncertainty on radios being tested. FM distortion is 1% and output level accuracy is ±1 dB for measurements down to −120 dBm.

The instrument can be modulated with an internal audio source that produces 10 Hz to 400 kHz signals. When wider bandwidths for modulating are required, it can use external sources ranging as high as 10 MHz. In fast-hopping mode, the maximum deviation is ±4 MHz. For measuring adjacent channel specifications such as selectivity and spurious response, the HP8645A has specified phase noise to −129 dBc at offsets of 20 kHz or greater. Spurious noise is 100 dB or more below the level of the carrier.

To test frequency-hopping and surveillance receivers, the signal generator can be synchronized either with a transmitter or directly to the receiver under test. Key receiver parameters such as hop rate, dwell time, amplitude, and frequency can be controlled precisely. Each amplitude setting can be set with ±1 dB accuracy.

The receiver's susceptibility to jamming can be tested by adjusting the amplitude of the signal generator's output. This feature allows the 8645A to effectively emulate a "follower jammer," which is a jamming device that locks onto and follows the frequency of the transmitted signal with a jamming signal.

Available now, the 8645A is delivered 10 weeks after order. – *Jonah McLeod*

Hewlett-Packard Co. Customer Information Center, 19310 Pruneridge Ave., Cupertino, Calif., 95014 [Circle 380]

PC-BASED EPLD TOOLS TARGET CMOS ONLY AND COST $1,000

By using personal computers as a platform and aiming solely at CMOS devices, Pistohl Electronics Tool Co. has come up with a development system for programmable, erasable logic devices that costs just $1,000. The system includes a logic assembler with an embedded 50-rule expert system, and its hardware can switch each of its 38 input/output lines on the fly without creating glitches in programming.

Tailoring the PET100 family family for CMOS chips avoided the costs involved in building systems that are to be used developing bipolar chips. Such systems generally require three voltage levels and special features to sense outputs signals, says Howard W. Johnson, the two-year-old-company's founder.

The Cupertino, Calif., company also took advantage of the personal-computer explosion by making the tools run on

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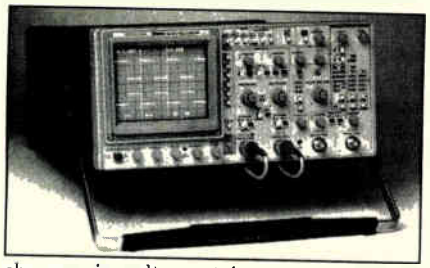

changes in voltage, trigger, and ground level for the wave form. It also stores up to 20 test setups and recalls them to the screen at the press of a button. Both scopes provide four channels, two of which are optimized for logic.

The 2245A costs $1,795 and the 2264A costs $2,395. Both of the models are available now.

Tektronix Inc., Portable Instruments Div., P.O. Box 1700, Beaverton, Ore., 97007.
Phone (800) TEK-WIDE [Circle 385]

PS/2 EXTENDER BOARD SPEEDS DEVELOPMENT

Tiara Computer Systems Inc.'s extender board lets hardware designers shorten development time for add-ons to IBM Corp.'s Personal System/2 computers, by allowing the prototype board to be removed from the computer housing for easy probe access.

The board features Micro Channel compatibility, four-layer pc-board noise immunity, shunts on +5-, +12-, and -12-V power lines, and over 21 sq. in. of prototyping area. All Micro Channel signals are available on header posts, each labeled according to its pin number on the connector. A logic ground reference is provided through a bus bar along the connector.

Available now, the PS/2 Extender costs $225.

Tiara Computer Systems Inc., 2700 Garcia Ave., Mountain View, Calif., 94043.
Phone (415) 965-1700 [Circle 389]

MEMORY TESTER RUNS UP TO 200 MHz

The T5481 memory tester from Advantest handles speeds up to 200-MHz VLSI memories and comes with two test heads.

The Advanced General-Purpose head provides 100-MHz testing capability. The Advanced ELC head can be used in multiplexed mode to test up to 200 MHz. The general-purpose head offers 2-ns output transition time at 3 V and 4.5-ns minimum pulse width over the full test clock range.

The ECL head boasts 0.5-ns output time and comparable pulse-width specifications. A wafer prober and autohandler interface are available options.

Up to 16 devices can be tested simultaneously with two test heads, and the system can handle up to eight 4-Mbit-by 1-bit dynamic random-access memories and static RAMs with 4- to 8-bit width at one time.

The T5481 is available now.

Advantest Inc., 300 Knightsbridge Pkwy., Lincolnshire, Ill., 60069.
Phone (312) 634-2552 [Circle 386]

80C86/80C88 EMULATORS OPERATE IN REAL TIME

Real-time, zero-wait-state emulation for the 16-bit 80C86 and 80C88 microprocessors sold by Intel Corp. and Harris Semiconductor Inc. is available for clock speeds of 8 MHz in the ES 1800 emulator from Applied Microsystems Corp.

The new emulator also includes a proprietary event monitor that provides powerful state-machine capabilities for triggering, breakpoint, and emulation control.

Options offered include a high-level language debugger and a software debugger. Both of these packages run on an IBM Corp. Personal Computer XT and AT or compatible machines. With them, engineers can debug in several high-level languages, among them C, Pascal, PL/M, Fortran, or Jovial.

The emulator also includes a Small Computer Systems Interface that allows data-transfer rates of 300 Kbytes/s.

Available now, the ES 1800 80C86/80C88 emulator costs $11,495.

Applied Microsystems Corp., 5020 148th Ave., NE, Redmond, Wash., 98073.
Phone (206) 882-2000 [Circle 387]

CAD TOOLS TARGET MIMIC DESIGNS

A set of microwave-circuit design-automation tools jointly developed by Ecad Inc. and Compact Software Corp., Patterson, N. J., provide designers with a means of drastically reducing design times for the Department of Defense's Mimic (Microwave Millimeter Wave IC) program.

Present microwave designs require manually interfacing and checking each step of a design. MiSym automates these functions.

The MiSym package includes tools for every stage of Mimic circuit design from schematic capture through physical layout. It also offers a direct interface to other microwave-simulation packages and incorporates a common user interface across all its packages.

MiSym is available now for Digital Equipment Corp.'s MicroVAX computers as well as Apollo Computer Co. and Sun Microsystems Inc. work stations. Pricing depends on the platform chosen.

Ecad Inc., 2455 Augustine Dr., Santa Clara, Calif., 95054.
Phone (408) 727-0264 [Circle 388]

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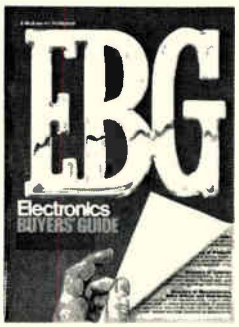

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ELECTRONICS WEEK

2ND $1 BILLION MONTH FOR U. S. CHIP ORDERS

The Semiconductor Industry Association says U. S. chip demand is holding steady and strong. The January book-to-bill ratio stayed even with December's at 1.13, and bookings crossed the $1 billion mark for the second straight month—the first time the SIA has recorded back-to-back billion-dollar months since 1984. But the news wasn't all good: bookings slipped 2.9% to $1.006 billion and billings suffered a 12.2% drop to $850.7 million. The slight downturn casts some doubt about the semiconductor industry's high hopes for 1988.

CDC SETTLES ON ONE UNIX VERSION . . .

Control Data Corp. says it will be the first computer vendor to offer one version of Unix for everything from desk-top work stations to supercomputers. The Minneapolis company will begin offering a version of Unix System V that is compatible with Posix, the forthcoming portable operating system interface standard [*Electronics*, Feb. 4, 1988, p. 31], on its Cyber Series work stations and mainframes by the second half of next year. It will be the same version scheduled for release in the third quarter of 1988 on the family of ETA^{10} supercomputers, which are built by ETA Systems Inc., a subsidiary based in St. Paul, Minn.

. . . AND BEGINS WORK ON 100-Mbyte/s NET

Control Data Corp. will develop a high-speed fiber-optic communications link for its Cyber mainframe computers under an agreement with Fibronics International Inc. The agreement calls for Control Data to design an intelligent peripheral interface that will let its Cyber computers communicate over Fibronics's 100-Mbyte/s System Finex network. Finex is the Hyannis, Mass., company's implementation of the Fiber-optic Distributed Data Interface, or FDDI network standard.

FEDERMAN BECOMES VENTURE CAPITALIST

Irwin Federman is following a host of other Silicon Valley executives into the venture capital business. The former president of Monolithic Memories Inc. and current vice-chairman of Advanced Micro Devices Inc. is joining Dillon Read & Co. as managing director of the firm's Concord Partners office in Palo Alto, Calif.. But he's not quitting his post at AMD. W. J. Sanders III, AMD's chairman, says Federman will continue to chart AMD's "strategic and tactical directions."

JUDGE REFUSES TO DROP Z80 CASE

Zilog Inc. is claiming a key legal victory in a judge's refusal to dismiss its case against NEC Corp. In its action, Zilog seeks rescission of a 1983 pact that settled earlier infringement claims against the Tokyo company by swapping Z80 rights for NEC's V series of microprocessors. Zilog officials in Campbell, Calif., want to nullify the pact because NEC was later sued by Intel Corp., which claims the V series violates its microcode rights. While the Intel-NEC battle continues, Zilog has opted not to ship any V series parts. No date has been set for Zilog's case in the U. S. District Court for the Northern District of California.

APPLE SHIPS ITS UNIX FOR MAC II

A version of the Unix operating system that Apple Computer Inc., Cupertino, Calif., has developed for the Macintosh II personal computer is now shipping, with a handful of third-party application programs ready now and others promised. Software written for Unix System V.2.2 can be ported to A/UX fairly easily, Apple says. The company has married Unix to the friendly Macintosh user interface, which makes A/UX unique in the Unix world. But the 2.2 version it is based upon is not the current standard—version 3.0—so Apple still has more catching up to do.

HITACHI WILL MAKE DRAMS IN U. S.

Hitachi Ltd. plans to make dynamic random-access memories in the U. S., and has resumed construction on a front-end wafer line in Irving, Texas. The fab was put on hold in 1986 during the DRAM market collapse. But with demand and prices rising, Hitachi's interest has peaked again. Full-scale production of 256-Kbit chips is expected to start in May 1989, using a 1.3-μm CMOS process. Hitachi may eventually also use the new wafer fabrication line to build logic products, such as microprocessors and application-specific integrated circuits.

SPIRE'S SOLAR CELL IS 21.7% EFFICIENT

In the leapfrogging competition to improve space-based solar cell efficiency, Spire Corp. has taken the lead with a gallium arsenide-on-germanium cell that proved 21.7% efficient in simulated space conditions. The previous record for space-based solar cells was 19.4%. On Earth, the 2-by-2-cm cells do even better—24.3%. By using germanium as a substrate, the Bedford, Mass., firm was able to make thinner, lighter cells with two junctions, one in each layer.

SONY TAKES AIM AT U. S. CAD MARKET

Sony Corp. is gunning for a share of the U. S. work station market. The company has set up a new unit, Sony Microsystems Co., to market NEWS, for Net Work Station, a 32-bit Unix-based engineering work station [*Electronics*, March 19, 1987, p. 79]. The $4,000 work station is priced well below offerings from Sun Microsystems Inc., which is a leading player in the two markets that Sony is most interested in: design systems for software and technical publishing. Unit president Masahiro Morimoto says the company expects to recruit 200 independent U. S. software vendors to develop application programs for NEWS.

MCC SUPERCONDUCTOR STUDY HAS 13 BACKERS

Thirteen companies have joined the Microelectronics and Computer Technology Corp.'s research study into electronic applications of high-temperature superconductivity. MCC began studying the materials last summer, concentrating on using high-temperature supercomputers as interconnects in super-cooled computers. Future work will include thin-film deposition and superconducting micro-chips.

TANDEM WILL USE MIPS'S RISC CHIP

Future work stations from Tandem Computers Inc. will use a reduced-instruction-set computer architecture designed by MIPS Computer Systems Inc. Executives at Tandem's Micro Products Division in Austin, Texas, decline to say when the company will introduce the RISC-based systems, which use AT&T Co.'s Unix System V operating system. The new work stations are expected to replace Tandem's year-old LXN system. Tandem's choice of MIPS is a big win for the Sunnyvale, Calif., company, which is battling an emerging field of other RISC vendors in a race to line up customers.

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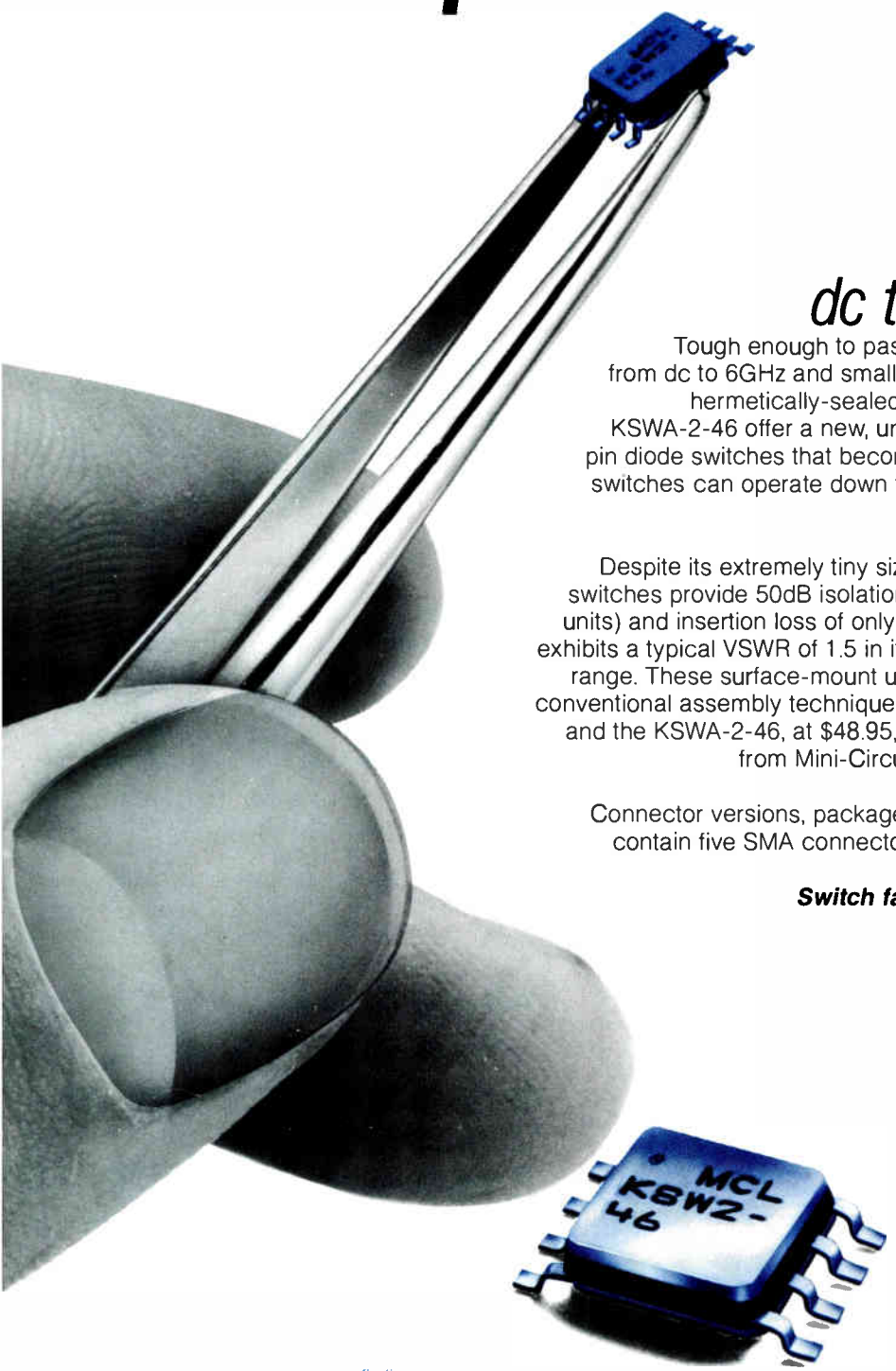

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INSERT. LOSS (db)		typ	max	typ	max
dc-200MHz		0.9	1.1	0.8	1.1
200-1000MHz		1.0	1.3	0.9	1.3
1-4.6GHz		1.3	1.7	1.5	2.6
ISOLATION (dB)		typ	min	typ	min
dc-200MHz		60	50	60	50
200-1000MHz		45	40	50	40
1-4.6GHz		30	23	30	25
VSWR (typ)	ON	1.3:1		1.3	
	OFF	—		1.4	
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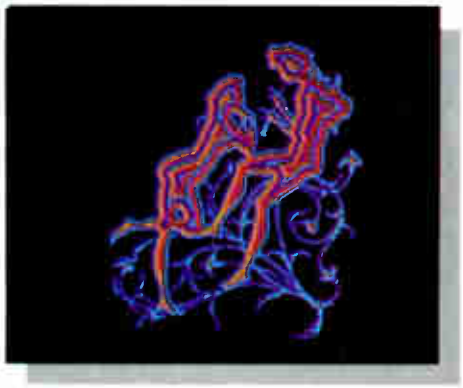

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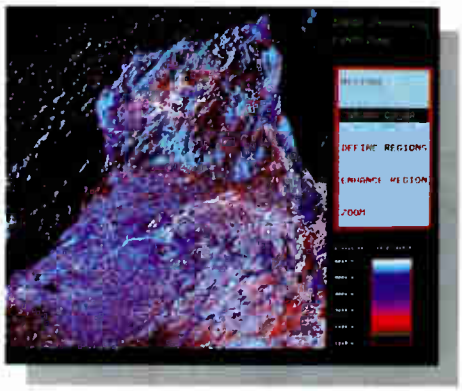

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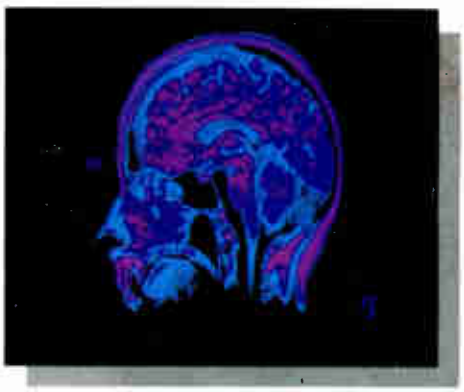

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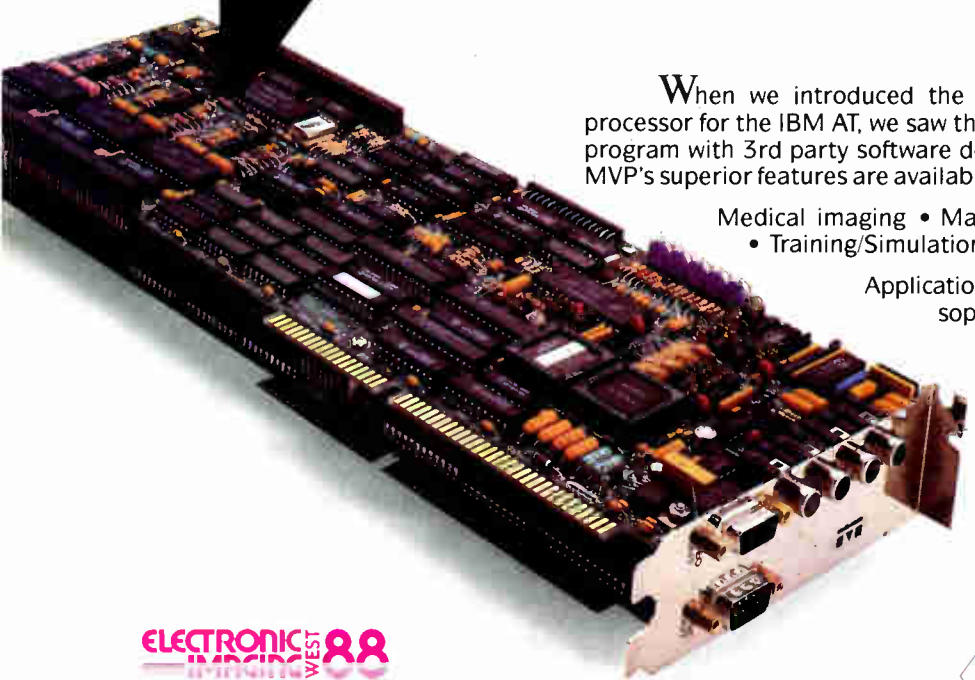

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